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# LHC

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**LHC-MPP-HCP-0006**

Date: 2016-01-08

MP3 Procedure

# Test Procedure and Acceptance Criteria for the 60 A Circuits

ABSTRACT:

This document describes the test procedure and the acceptance parameter specification for the 60 A circuits. A list of the parameters to acquire during the tests is given.

| PREPARED BY: | CHECKED BY: | APPROVED BY: |
|---|---|---|
| MP3 | MP3<br>Odd Andreassen<br>Amalia Ballarino<br>Jean-Christophe Garnier<br>Mirko Pojer<br>Felix Rodriguez-Mateos<br>Rüdiger Schmidt<br>Matteo Solfaroli Camillocci<br>Yves Thurel<br>Jorg Wenninger<br>Markus Zerlauth | Luca Bottura<br>Jean-Paul Burnet<br>Dimitri Delikaris<br>Mike Lamont<br>Andrzej Siemko |

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# HISTORY OF CHANGES

| REV. NO. | DATE | PAGES | DESCRIPTIONS OF THE CHANGES |
|---|---|---|---|
| 0.1 | 2007-03-22 | 9 | First draft |
| | 2007-04-03 | 9 | First released document |
| | 2007-09-03 | 14 | Test procedure includes PCC and PNO3 tests |
| | 2007-09-10 | 14 | Analysis source added to Appendix3. Calculation of R_Lead clarified during PCC. Analysis of crowbar during PCC added. |
| | 2007-09-12 | 14 | Alignment of variable names |
| | 2007-09-13 | 15 | Addition of description column to table in Appendix3 (Variables to be stored) |
| | 2007-09-13 | 17 | Update to Main Cycle Test description. |
| | 2007-09-14 | 17 | Units in Appendix 3 table updated. |
| | 2007-09-14 | 17 | Title, abstract, failure investigation and names in Appendix 1 |
| | 2007-09-20 | 17 | MTF profile included. Parameter added to first ramp in PCC. New variable to be stored (I_ERR_PCC_RAMP). |
| | 2007-09-20 | 17 | Update of the description in case of test failure and corrected sign into PNO Offline analysis. |
| | 2007-09-26 | 17 | New point with the structure of the document. Addition of description column to table in Appendix1 (Test Parameters). Coherence between test names, LHC-MPP-HCP-0001 and LHC-D-HCP-0003 document and MTF steps. Minor changes in actions and parameters names. |
| | 2007-10-04 | 17 | 3. Test Cycle: updated for I_PCC_MID and naming convention<br>Appendix 1: value for I_MID_PCC corrected<br>Appendix 2 : clarification that circuits are examples<br>P7 and Appendix 3 : I_EARTH_PNO_POS and I_EARTH_PNO_NEG replace I_EARTH_PNO |
| | 2007-10-09 | 17 | Appendix 3: New column with the associated test of each variable. |
| | 2007-10-15 | All | Submission for engineering check |
| | 2008-01-11 | All | Replace Waiting time of 3 L/(R + R crowbar) by new parameter TIME_ACTIVATION from LSA DB (page 9 step 3, page 10 step 7 and in Appendix 1)<br>Replace step PNO.g (Current Lead performance) with PCL<br>TIME_PCC added to step 8 of PCC.1.<br>Failure investigation text modified. |
| | 2008-03-11 | 11-12-13 | Based on the experience of sector 4-5, change the criteria for U_LEAD_OFS from 2e-3 to 3.5e-3 V and R_MAGNET_PNO from 3e-3 to 3.5e-3 Ohm. |

| | | | |
|---|---|---|---|
| | 2008-03-11 | 17 | Adding a text file containing the PNO.A1 criteria at the moment of the test, to the MTF results. |
| 0.11 | 2008-03-11 | 7, 8, 9<br>12 – 15 | Update of criteria for I_ERR |
| 0.12 | 2008-03-12 | 14 | Added team responsibilities to the offline analysis section |
| | | 7 | Updated offline crowbar analysis criteria |
| | | 5 | Update of criteria for U_Lead_Offset criteria and I_PCC_MID |
| | | | Addition of restrictions for parallel testing during PCC |
| 0.2 | 2008-04-17 | | Submission for approval |
| 0.21 | 2008-05-06 | 7 | Changed the title from "The test cycle" to "The test sequence" |
| | | 17 | Changed what to do in case of failure from "If the failure is significant, the EIC should open an NC (non conformity), or ensure the specialist concerned opens an NC." to "If the failure is significant, the MP3 or TE-EPC expert should open an NC (non conformity)." |
| 1.0 | 2008-05-14 | All | Released |
| 1.1 | 2009-04-30 | All | Change on the acceleration of the PCC test from 0.5 A/s to 1 A/s to comply with the ECR LHC-MPP-EC-0001. |
| 1.2 | 2009-05-18 | All | Submission for approbation |
| 2.0 | 2009-06-16 | All | Released |
| 2.1 | 2010-11-24 | 24 | Add "Appendix 4" describing foreseen cases when the procedure or part of procedure must be applied |
| 2.2 | 2011-04-12 | All | Updates according to circulation and feedback given from checkers |
| | | 14 | Following MP3 wrap-up session, update criteria on final R_MAG |
| 3.0 | 2012-02-06 | - | Release for 2012 version. No changes |
| 3.1 | 2014-04-14 | All | General review of the document. Changes in the structure and the re-commissioning scenarios. Submitted for Approval |
| 4.0 | 2014-08-04 | All | Released |
| 4.1 | 2016-01-08 | 6-10 | Update of the document for HWC during YETS 2015. |
| | | | Minor formatting modifications. |

# TABLE OF CONTENTS

# 1. INTRODUCTION

This Hardware Commissioning (HWC) procedure describes the test sequence, test parameters, analysis, and validation criteria for the powering tests of the 60A circuits of the LHC. A brief description of the circuit and the signals is given in section 2. An overview of the tests is given in section 3. The sequence of tests to be performed is described in section 4.

Each individual test, along with the required analysis and signatures, is described in section 5. The sequencer steps for each test are detailed in Appendix 2. Online analysis is performed by the sequencer based on criteria defined by the experts, see also Appendix 2. A detailed description of the offline analysis is documented on the MP3 website (cern.ch/MP3). Offline analysis and test validation is performed by experts from various teams.

Throughout all the tests, the basic cryogenic conditions for operation must be assured through the 60 A software Power Permit system. The conditions that are used to interlock the Power_Permit signal are defined as:

- main magnet temperature in the whole arc <4 K,
- beam screen temperature along whole arc <30 K.

However it is noted that the magnets should be tested as close to nominal conditions as possible (thus 1.9 K).

Throughout this procedure the following abbreviations are used:

| | |
|---|---|
| **CL:** | Current Leads (Responsible) |
| **PIC:** | PIC (Team) |
| **CRYO:** | Cryogenics (Team) |
| **NC:** | Non-conformity |
| **PC:** | Power Converter (Team) |
| **PM:** | Post Mortem |
| **MP3:** | Magnet circuits, powering and performance panel |

# 2. CIRCUIT AND SIGNAL DESCRIPTION

The LHC comprises a total of 376 pairs of horizontal and vertical orbit correctors which are installed at each focusing and defocusing main quadrupole magnet in the arcs. Quenches on 60 A magnets are detected by the power converter through magnet impedance growing. In addition, the power converter also provides current lead protection. Figure 1 shows the circuit diagram of the 60 A arc orbit correctors.

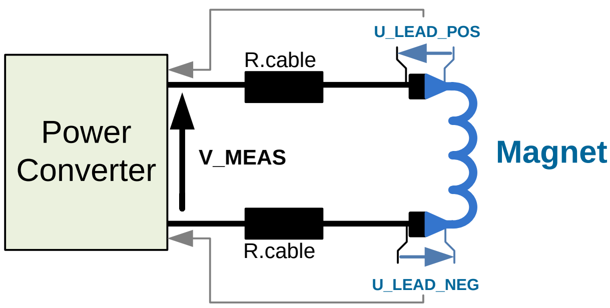



Figure 1 – Simplified circuit schematic

In order to power the 60 A orbit correctors a global permit signal is transmitted via the controls and the timing system to all converters in each of the eight LHC sectors when all conditions for powering in the long arc cryostat are met. Figure 2 shows the interlock transmission logic (see EDMS 944765).

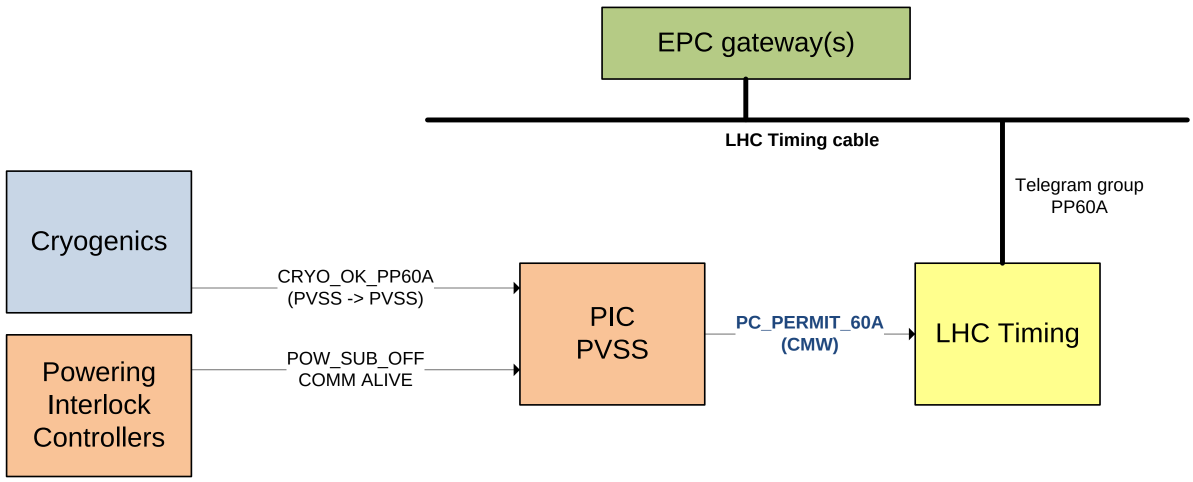



Figure 2 – 60 A Powering Permit transmission

# 3. SUMMARY OF THE TESTS

The entire test is made of the following steps, sorted by current level:

| | |
|---|---|
| **PCC.1** | Converter Configuration 4Q |
| **PNO.d1** | Bipolar Powering Failure at ±(I_PNO+I_DELTA) |
| **PNO.a1** | Bipolar Cycle to ±I_PNO |

The test should start with the execution of the **PCC.1** test and the test must be passed, including the offline analysis by a TE-EPC expert. When testing multiple systems in parallel, PCC should be separately made on the H and V systems.
Following this approval the **PNO.d1** tests can be performed, followed by an offline analysis. Upon approval of the **PNO.d1** test one can proceed with the **PNO.a1** test.
At the end, in order to validate the circuit, the three steps **PCC.1**, **PNO.a1** and **PNO.d1** must have been completed successfully. A list of variables will then be stored in MTF to characterise the circuit.

The following table summarizes the tests to be carried out for each circuit, as well as the teams that have to perform the analysis. More information on each type of analysis can be found in section 5.

| Test name | MP3 | PC |
|---|---|---|
| **PCC.1** | | ■ |
| **PNO.d1** | ■ | ■ |
| **PNO.a1** | ■ | |

If a test fails, the failure should be reported to the EIC, who will consult the PC and/or MP3 specialists to decide on the best action. It may be necessary to proceed with further investigations to find the source of the failure. If the failure is significant, the MP3 or PC expert should open a NC (non-conformity).

# 4. TEST SEQUENCE MATRIX

Table 1 shows the tests that have been performed for previous HWC campaigns and that will be performed for the upcoming campaign. Included is also a set of tests to be performed in case of warm-up of the sector.

Table 1 – Tests to be performed (indicated in blue) for different HWC campaigns or other situations.

| | PCC.1 | PNO.d1 | PNO.a1 |
|---|---|---|---|
| Warm up of the circuit above 90 K | | | |
| Technical stop > 3 weeks | | | |
| HWC 2008 | | | |
| HWC 2014 | | | |

# 5. TEST DESCRIPTION

## 5.1 PCC.1: POWER CONVERTER CONFIGURATION 4Q

The aim of this test is to validate the configuration and the performance of the power converter. It also checks the crowbar activation at low current.

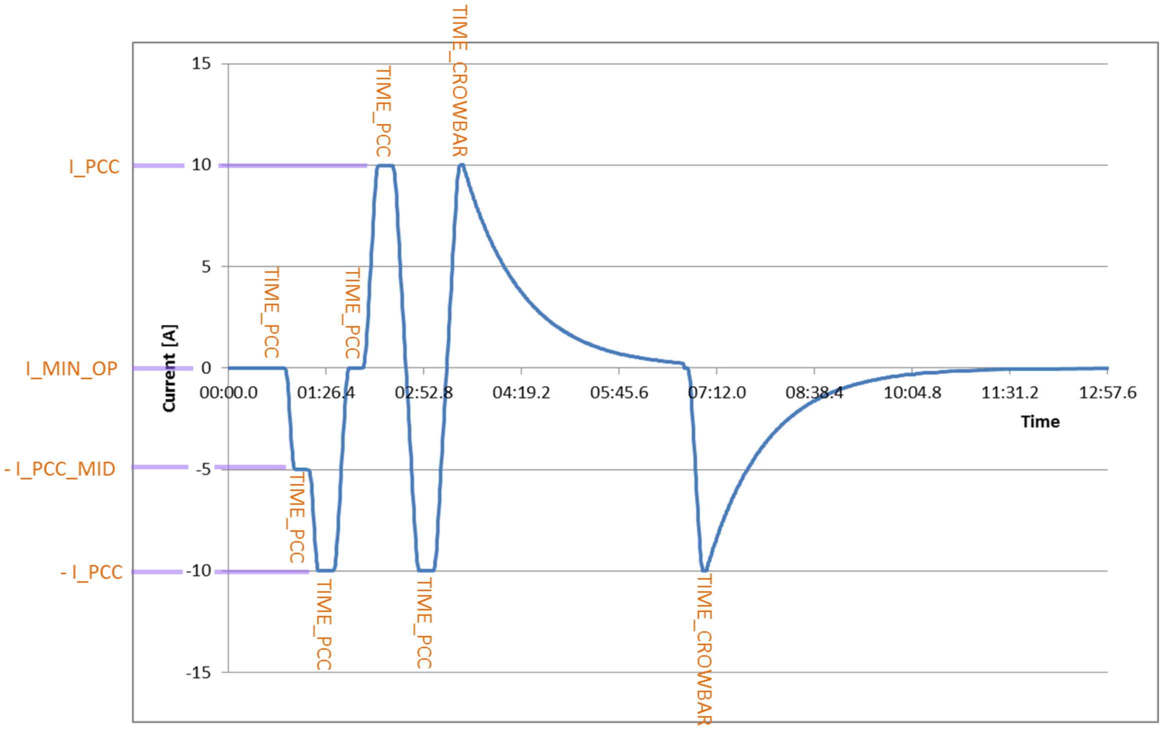



Figure 3 – Current cycle during PCC.1

The offline analysis is listed below:

| Responsible | Type of analysis | Criteria |
|---|---|---|
| PC | Verify the converter current I_MEAS after the crowbar activation for both bipolar cycles | **\|I_MEAS\|@60s = +3.7A±0.6A** |
| PC | Verify that the exponential decay of I_MEAS and V_MEAS is within tolerance for both bipolar cycles | **\|Tolerance(I_MEAS)\|<=1A<br>\|Tolerance(V_MEAS)\|<=0.1V** |

## 5.2 PNO.D1: BIPOLAR POWERING FAILURE (I_PNO + I_DELTA)

This test verifies the correct behaviour of the crowbar at nominal current following a powering failure. This test will be done at I_PNO + I_DELTA to ensure that the magnets are trained to a margin above I_PNO and to avoid quenches at flattop.

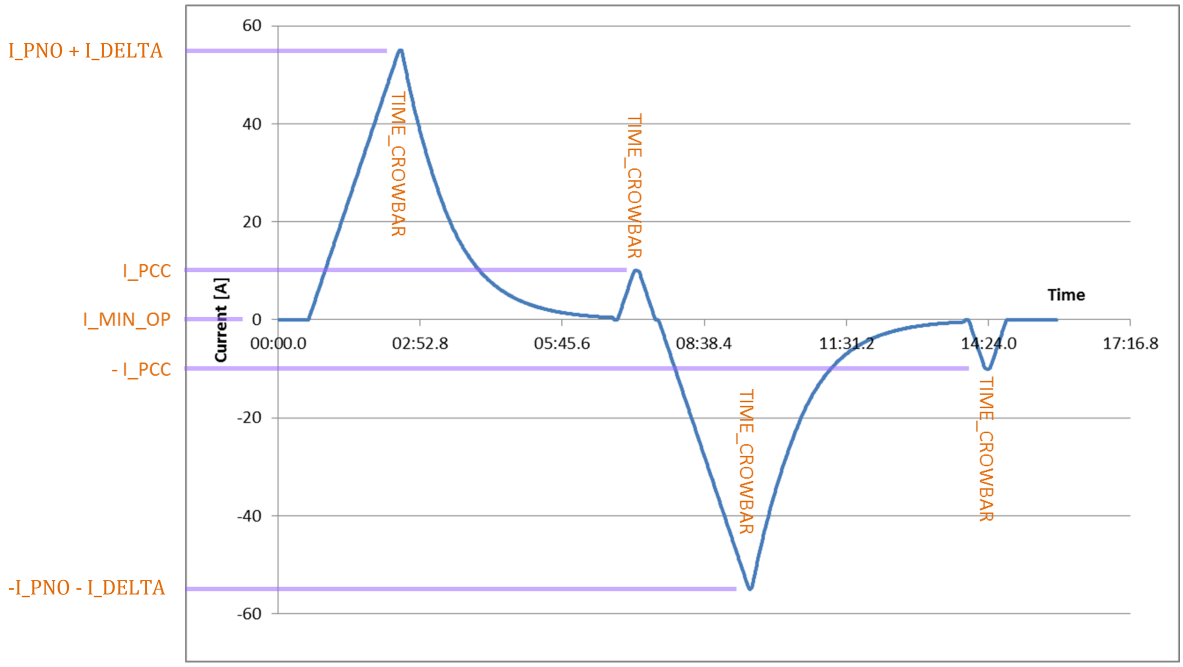



Figure 4 – Current cycle during PNO.d1

The offline analysis for the +I_PNO cycle is listed below:

| Responsible | Type of analysis | Criteria |
|---|---|---|
| PC | Verify the time duration after the crowbar activation when V_MEAS is no longer -1.1V±0.1V | **60s±10s** |
| PC | Verify that converter current is within range when the converter voltage is no longer -1.1V±0.1V | **I_MEAS = +23A±5A** |
| PC | Verify the converter current 120s after the crowbar activation | **I_MEAS@120s =+8A±2A** |
| PC | Verify that the exponential decay of I_MEAS and V_MEAS is within tolerance | **\|Tolerance(I_MEAS)\|<=2A<br>\|Tolerance(V_MEAS)\|<=0. 15V** |

The offline analysis for the -I_PNO cycle is listed below:

| Responsible | Type of analysis | Criteria |
|---|---|---|
| PC | Verify the time duration after the crowbar activation when V_MEAS is no longer +1.1V±0.1V | **60s±10s** |
| PC | Verify that converter current is within range when the converter voltage is no longer +1.1V±0.1V | **I_MEAS = -25A±5A** |
| PC | Verify the converter current 120s after the crowbar activation | **I_MEAS@120s =-8A±2A** |
| PC | Verify that the exponential decay of I_MEAS and V_MEAS is within tolerance | **\|Tolerance(I_MEAS)\|<=2A \|Tolerance(V_MEAS)\|<=0.15V** |

## 5.3 PNO.A1: BIPOLAR CYCLE (±I_PNO)

This test verifies the correct behaviour of the magnets and current leads at nominal current.

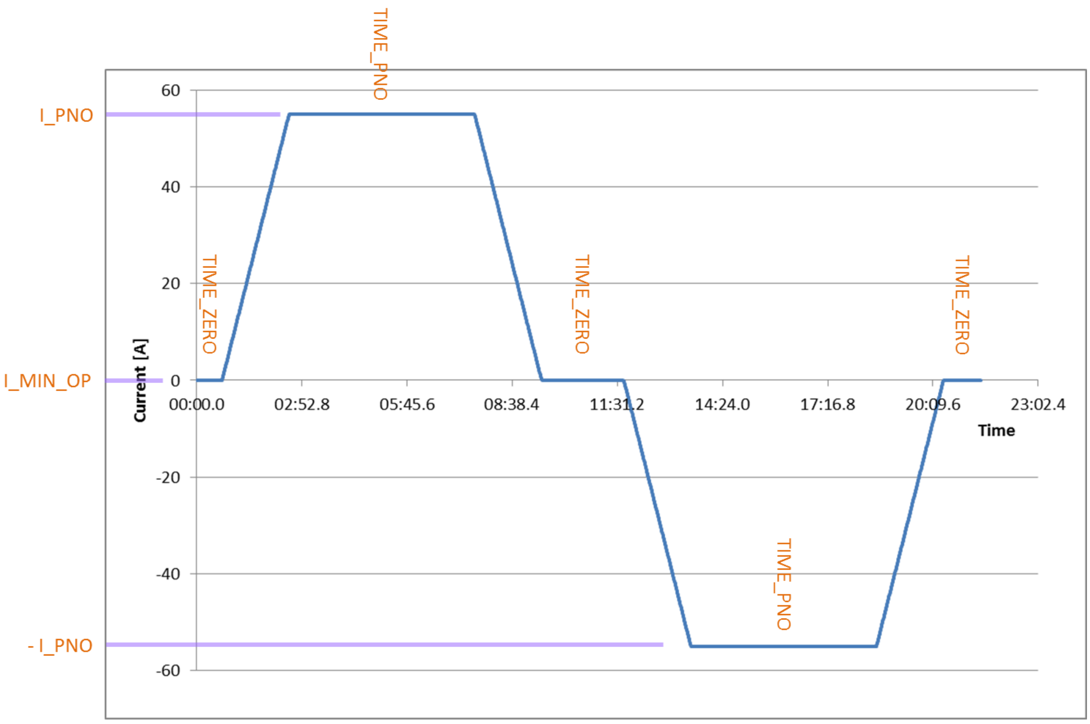



Figure 5 – Current cycle during PNO.a1

The offline analysis is listed below:

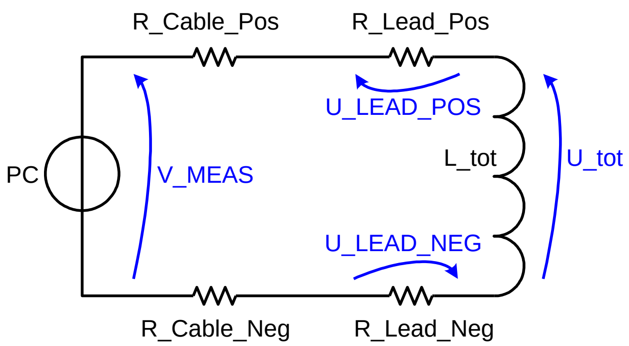
| Responsible | Type of analysis | Criteria |
|---|---|---|
| MP3 | Verify the offset voltage for both POS and NEG leads at I_MIN_OP | **\|U_LEAD_NEG\| <= 3.5mV**<br>**\|U_LEAD_POS\| <= 3.5mV** |
| MP3 | Verify the maximum current lead voltage at both ± I_PNO | **\|U_LEAD_NEG\| = 50mV±25mV**<br>**\|U_LEAD_POS\| = 50mV±25mV** |
| MP3 | Verify the current lead resistance during both positive and negative cycles | **R_LEAD_POS = 0.4mOhm±50%**<br>**R_LEAD_NEG = 0.4mOhm±50%** |
| MP3 | Verify the slope of the resistance change with time at I_PNO during both positive and negative cycles | **DRDT_LEAD_POS <1.8uOhm/s**<br>**DRDT_LEAD_NEG <1.8uOhm/s** |
| MP3 | Evaluate the circuit inductance during both positive and negative cycles | **L_CIRCUIT = 2.8H±0.3H** |
| MP3 | Magnet resistance by subtracting the cable voltage (I_MEAS*V_MEAS) and the leads voltage from the converter voltage during both positive and negative cycles | **R_MAGNET < 3mOhm** |
| MP3 | Evaluate the average offset between the reference and the measured voltage. Record the maximum offset during both positive and negative cycles | **\|U_PC_OFFSET\|<50mV** |
| MP3 | Average of magnet resistance during positive and negative cycle | **(R_MAGNET_PNO_POS+ R_MAG_PNO_NEG)/2** |

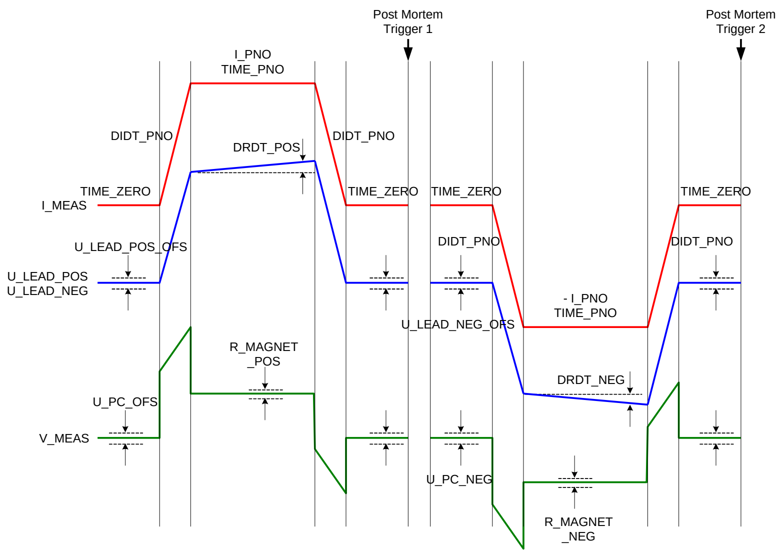
# 6. APPENDICES

## 6.1 APPENDIX 1: TEST PARAMETERS

The following parameters are valid for all circuits unless otherwise noted in the list of exceptions (see LHC-MPP-HCP-0103 EDMS Number 1375861)

| Parameter | Value | Unit | Description |
|---|---|---|---|
| I_PCC | 10 | A | Maximum current used in PCC |
| I_PCC_MID | 5 | A | Intermediate current used in PCC |
| I_PNO | 55 | A | Nominal current |
| I_DELTA | 5 | A | Current margin for training beyond I_PNO |
| I_MIN_OP | 0 | A | Minimum operational current |
| I_EARTH_PCC_MAX | 0.005 | A | Maximum earth leakage on PC during PCC |
| I_EARTH_PNO_MAX | 0.005 | A | Maximum earth leakage on PC during PNO |
| I_ERR_MAX | 0.0042 | A | Maximum error on current measurement |
| R_LEAD_MAX | 0.00135 | Ohm | Maximum acceptable resistance value for CL |
| R_LEAD_MIN | 0.00045 | Ohm | Minimum acceptable resistance value for CL |
| DIDT_PNO | 0.5 | A/s | Nominal current ramp rate |
| DIDT_PCC | 1 | A/s | Current ramp rate used in PCC |
| ACC_PNO | 0.25 | A/s2 | Nominal current acceleration |
| TIME_PNO | 300 | s | Time for the flat-tops at I_PNO |
| TIME_ZERO | 30 | s | Time for the flat-tops at I_MIN_OP |
| TIME_PCC | 10 | s | Time for the flat-tops in PCC |
| TIME_CROWBAR | 2 | s | Time interval used in the crowbar tests |
| TIME_ACTIVATION | LSA | s | Time since activation > 3 L/(R + Rcrowbar) |
| U_LEAD_MAX | 0.0035 | V | Maximum acceptable voltage on CL |



## 6.2 APPENDIX 2: TEST SEQUENCES

### 6.2.1 APPENDIX 2.1: PCC.1 POWER CONVERTER CONFIGURATION 4Q

During this step, the configuration and the performance of the power converter are checked.

| Step | Description | Criteria |
|---|---|---|
| 1 | Check the converter configuration. The converter or database configuration may be updated as part of this process. | EPC ensures that the converter is configured. |
| 2 | Start the power converter. Once in standby, initiate a converter fault to create a post-mortem event. | Check that the PM file PM_STARTUP_PCC exists |
| 3 | Start the converter and wait TIME_PCC at I_MIN_OP. Measure the current lead offset. Remove the offset from all subsequent measurements. | \|U_LEAD\|<U_LEAD_MAX |
| 4 | Ramp the converter to -I_PCC_MID at DIDT_PCC and ACC_PNO. | |
| 5 | Wait TIME_PCC at -I_PCC_MID. | |
| 6 | Ramp the converter to -I_PCC at DIDT_PCC and ACC_PNO. | |
| 7 | Reset the U_LEAD buffers. Wait TIME_PCC at -I_PCC. Obtain the converter maximum lead voltage and maximum absolute current error. | For both POS and NEG:<br>R_LEAD_XXX_PCC =<br>(U_LEAD_XXX_PCC_NEG-<br>U_LEAD_XXX_OFS_PCC_POS)/I_PCC =<br>0.9mOhm ± 50%<br>I_ERR <I_ERR_MAX |
| 8 | Ramp the converter to I_MIN_OP at DIDT_PCC and ACC_PNO. Wait TIME_PCC at I_MIN_OP. | |
| 9 | Ramp the converter to I_PCC at DIDT_PCC and ACC_PNO. | |
| 10 | Reset the U_lead buffers. Wait TIME_PCC at I_PCC. Obtain the converter maximum lead voltage. | For both POS and NEG:<br>R_LEAD_XXX_PCC_POS =<br>(U_LEAD_XXX_PCC_POS –<br>U_LEAD_XXX_OFS_PCC_POS)/I_PCC =<br>0.9mOhm ± 50% |
| 11 | Ramp the converter to -I_PCC at DIDT_PCC and ACC_PNO. | |
| 12 | Wait TIME_PCC at –I_PCC. | |
| 13 | Ramp the converter to I_PCC at DIDT_PCC and ACC_PNO. At the end of the ramp obtain the converter maximum earth current, and maximum absolute current error. | I_EARTH <I_EARTH_PCC_MAX<br><br>I_ERR <I_ERR_MAX |
| 14 | Wait TIME_CROWBAR at I_PCC. | |
| 15 | Activate the crowbar by setting a converter power failure (FGC_STATE fault). Record the name of the post-mortem file that is created. | Check that the PM file PM_CROWBAR_POS exists |
| 16 | Wait until all the following conditions are true:<br>1. PC is FAULT_OFF or OFF<br>2. Wait TIME_ACTIVATION<br>3. I_MEAS < 1A<br>4. PM has finished sending data | Check that only FGC_STATE fault is present |
| 17 | Start the converter and ramp to -I_PCC at DIDT_PCC and ACC_PNO. Wait TIME_CROWBAR at -I_PCC.<br>Then, acquire the PC faults. | |
| 18 | Activate the crowbar by setting a converter power failure (FGC_STATE fault). Record the name of the post-mortem file that is created. | Check that the PM file PM_CROWBAR_NEG exists |

| | | |
|---|---|---|
| 19 | Wait until all the following conditions are true:<br>1. PC is FAULT_OFF or OFF<br>2. Wait TIME_ACTIVATION<br>3. I_MEAS < 1A<br>4. PM has finished sending data | Check that only FGC_STATE fault is present |

### 6.2.2 APPENDIX 2.2: PNO.D1 BIPOLAR POWERING FAILURE

| Step | Description | Criteria |
|---|---|---|
| 1 | Turn the PC to standby | |
| 2 | Ramp to I_PNO+I_DELTA at DIDT_PNO and ACC_PNO. Wait TIME_CROWBAR, then initiate a converter fault (FGC_STATE fault) to trigger the post-mortem acquisition. | Check that the PM file PM_CROWBAR_PNO_POS exists |
| 3 | Wait until all the following conditions are true:<br>1. PC is FAULT_OFF or OFF<br>2. Wait TIME_ACTIVATION<br>3. I_MEAS < 1A<br>4. PM has finished sending data<br>Then, acquire the PC faults. | Check that only FGC_STATE fault is present |
| 4 | Turn on the converter and ramp the current to +I_PCC at DIDT_PNO and ACC_PNO, wait TIME_CROWBAR, ramp to I_MIN_OP at DIDT_PNO and ACC_PNO | Ramp successful (no PC fault) |
| 5 | Ramp to<br>-I_PNO-I_DELTA at DIDT_PNO and ACC_PNO. Wait TIME_CROWBAR, then initiate a converter fault (FGC_STATE fault) to trigger the post-mortem acquisition. | Check that the PM file PM_CROWBAR_PNO_NEG exists |
| 6 | Wait until all the following conditions are true:<br>1. PC is FAULT_OFF or OFF<br>2. Wait TIME_ACTIVATION<br>3. I_MEAS < 1A<br>4. PM has finished sending data<br>Then, acquire the PC faults. | Check that only FGC_STATE fault is present |
| 7 | Turn on the converter and ramp the current to -I_PCC at DIDT_PNO and ACC_PNO, wait TIME_CROWBAR, ramp to I_MIN_OP at DIDT_PNO and ACC_PNO | Ramp successful (no PC fault) |

### 6.2.3 APPENDIX 2.3: PNO.A1 BIPOLAR CYCLE

| Step | Description | Criteria |
|---|---|---|
| 1 | Turn on the converter and wait at least TIME_ZERO at I_MIN_OP. | |
| 2 | Ramp the current to I_PNO at DIDT_PNO and ACC_PNO. | |
| 3 | Reset the converter maximum I_earth buffer. Wait at least TIME_PNO at I_PNO.<br>Acquire I_EARTH. | I_EARTH<I_EARTH_PNO_MAX |
| 4 | Ramp the current to I_MIN_OP at DIDT_PNO and ACC_PNO. | |
| 5 | Wait at least TIME_ZERO at I_MIN_OP. After waiting acquire converter maximum absolute current error. | I_ERR<I_ERR_MAX |
| 6 | Initiate a converter fault (FGC_STATE fault) to trigger the post mortem acquisition. | Check if PM file PM_CYCLE_PNO_POS exists |
| 7 | Turn on the converter and wait at least TIME_ZERO at -I_MIN_OP. | |

| | | |
|---|---|---|
| 8 | Ramp the current to<br>-I_PNO at DIDT_PNO and ACC_PNO. | |
| 9 | Reset the converter maximum I_earth buffers. Wait at least TIME_PNO at -I_PNO.<br>Acquire I_EARTH. | I_EARTH<I_EARTH_PNO_MAX |
| 10 | Ramp the current to I_MIN_OP at DIDT_PNO and ACC_PNO. | |
| 11 | Wait at least TIME_ZERO at I_MIN_OP. After waiting acquire converter maximum absolute current error. | I_ERR<I_ERR_MAX |
| 12 | Initiate a converter fault (FGC_STATE fault) to trigger the post mortem acquisition. | Check if PM file PM_CYCLE_PNO_NEG exists |

## 6.3 APPENDIX 3: MTF PROFILE

This is the MTF profile for the 60 A circuits:
095-HCA PCC.1 Converter Configuration 4Q
701-HCA PNO.a1 Bipolar Cycle I_PNO
731-HCA PNO.d1 Bipolar Powering Failure

## 6.4 APPENDIX 4: VARIABLES USED FOR ANALYSIS

The parameters below are given for an example circuit, RPLA.12L8.RCBH11.L8B1. The same parameters can be found for other circuits by changing the circuit name.

| Description | Parameter name | Source |
|---|---|---|
| Current measurement of RPLA.12L8.RCBH11.L8B1 | RPLA.12L8.RCBH11.L8B1:**I_MEAS** | PM |
| Voltage measurement of RPLA.12L8.RCBH11.L8B1 | RPLA.12L8.RCBH11.L8B1:**V_MEAS** | PM |
| Voltage across current lead at low polarity voltage tap of RPLA.12L8.RCBH11.L8B1 | RPLA.12L8.RCBH11.L8B1:**U_LEAD_NEG** | PM |
| Voltage across current lead at high polarity voltage tap of RPLA.12L8.RCBH11.L8B1 | RPLA.12L8.RCBH11.L8B1:**U_LEAD_POS** | PM |
| Calculated ratio U_LEAD_NEG/I_MEAS of RPLA.12L8.RCBH11.L8B1 | RPLA.12L8.RCBH11.L8B1:**R_LEAD_NEG** | PM |
| Calculated ratio U_LEAD_POS/I_MEAS of RPLA.12L8.RCBH11.L8B1 | RPLA.12L8.RCBH11.L8B1:**R_LEAD_POS** | PM |
| Inductance of the circuit RPLA.12L8.RCBH11.L8B1 | RPLA.12L8.RCBH11.L8B1:**L_TOT** | LHC Functional Layout Database |
| Warm cable resistance of RPLA.12L8.RCBH11.L8B1 | RPLA.12L8.RCBH11.L8B1:**R_TOT** | LHC Functional Layout Database |
| Measured warm cable resistance of RPLA.12L8.RCBH11.L8B1 | RPLA.12L8.RCBH11.L8B1:**R_TOT_MEASURED** | LHC Functional Layout Database |
| Maximum ground current on load side measured by the converter of RPLA.12L8.RCBH11.L8B1 | RPLA.12L8.RCBH11.L8B1:<br>**MEAS.MAX_I_EARTH** | FGC |
| Maximum lead voltage measured by the converter of RPLA.12L8.RCBH11.L8B1 | RPLA.12L8.RCBH11.L8B1:<br>**MEAS.MAX_U_LEADS [0]**<br>RPLA.12L8.RCBH11.L8B1:<br>**MEAS.MAX_U_LEADS [1]** | FGC |

| | | |
|---|---|---|
| Maximum error between reference and measured value at loop sampling speed | RPLA.12L8.RCBH11.L8B1: **ILOOP.MAX_ABS_ERR** | FGC |

## 6.5 APPENDIX 5: VARIABLES TO BE STORED

| Parameter | Unit | Analysis Source | Description | Test | To be filled by |
|---|---|---|---|---|---|
| TEST_PROCEDURE_VERSION | Text / hyperlink | Offline | EDMS version number of the test procedure applied. | None | MP3 |
| TEST_CRITERIA_PNO_A1 | Text file | Offline | Text file containing the criteria applied at the moment of PNO.A1 validation | PNO.A1 | MP3 |
| PM_STARTUP_PCC | Text / hyperlink | Online | Postmortem filename of PC startup sequence | PCC.1 | PMA |
| U_LEAD_POS_OFS_PCC_POS | V | Online | Voltage offset of POS current lead measured during PCC | PCC.1 | Sequencer |
| U_LEAD_NEG_OFS_PCC_POS | V | Online | Voltage offset of NEG current lead measured during PCC | PCC.1 | Sequencer |
| U_LEAD_POS_PCC_NEG | V | Online | Max voltage of POS current lead measured continuously at 50Hz during PCC POS flat-top | PCC.1 | Sequencer |
| U_LEAD_NEG_PCC_NEG | V | Online | Max voltage of NEG current lead measured continuously at 50Hz during PCC POS flat-top | PCC.1 | Sequencer |
| U_LEAD_POS_PCC_POS | V | Online | Max voltage of POS current lead measured continuously at 50Hz during PCC NEG flat-top | PCC.1 | Sequencer |
| U_LEAD_NEG_PCC_POS | V | Online | Max voltage of NEG current lead measured continuously at 50Hz during PCC NEG flat-top | PCC.1 | Sequencer |
| R_LEAD_POS_PCC | Ohm | Online | Max POS lead resistance calculated during PCC flat-top | PCC.1 | Sequencer |
| R_LEAD_NEG_PCC | Ohm | Online | Max NEG lead resistance calculated during PCC flat-top | PCC.1 | Sequencer |
| I_EARTH_PCC | A | Online | Max earth current measured during PCC | PCC.1 | Sequencer |
| I_ERR_PCC | A | Online | Max error between current reference and measured current during PCC, acquired continuously by the PC at the speed of the current loop | PCC.1 | Sequencer |
| I_ERR_PCC_RAMP | A | Online | Max error between current reference and measured current during | PCC.1 | Sequencer |

| | | | | | |
|---|---|---|---|---|---|
| | | | the first negative ramp in PCC without crossing 0A. Acquired continuously by the PC at the speed of the current loop | | |
| PM_CROWBAR_PCC_POS | Text / hyperlink | Online | Postmortem filename of POS current PCC crowbar activation | PCC.1 | PMA |
| PCFLT_PWR_FAIL_PCC_POS | Text | Online | Converter faults after POS current PCC crowbar activation. | PCC.1 | Sequencer |
| PM_CROWBAR_PCC_NEG | Text / hyperlink | Online | Postmortem filename of NEG current PCC crowbar activation | PCC.1 | PMA |
| PCFLT_PWR_FAIL_PCC_NEG | Text | Online | Converter faults after NEG current PCC crowbar activation. | PCC.1 | Sequencer |
| I_EARTH_PNO_POS | A | Online | Max earth current measured during POS PNO flat-top. | PNO.A1 | Sequencer |
| I_EARTH_PNO_NEG | A | Online | Max earth current measured during NEG PNO flat-top. | PNO.A1 | Sequencer |
| I_ERR_PNO_POS | A | Online | Max error between current reference and measured current during POS PNO cycle, acquired continuously by the PC at the speed of the current loop | PNO.A1 | Sequencer |
| I_ERR_PNO_NEG | A | Online | Max error between current reference and measured current during NEG PNO cycle, acquired continuously by the PC at the speed of the current loop | PNO.A1 | Sequencer |
| PM_CYCLE_PNO_POS | Text / hyperlink | Online | Postmortem filename of POS PNO cycle | PNO.A1 | PMA |
| PM_CYCLE_PNO_NEG | Text / hyperlink | Online | Postmortem filename of NEG PNO cycle | PNO.A1 | PMA |
| PM_CROWBAR_PNO_POS | Text / hyperlink | Online | Postmortem filename of POS current PNO crowbar activation | PNO.D1 | PMA |
| PCFLT_PWR_FAIL_PNO_POS | Text | Online | Converter faults after POS current PNO crowbar activation. | PNO.D1 | Sequencer |
| PM_CROWBAR_PNO_NEG | Text / hyperlink | Online | Postmortem filename of NEG current PNO crowbar activation | PNO.D1 | PMA |
| PCFLT_PWR_FAIL_PNO_NEG | Text | Online | Converter faults after NEG current PNO crowbar activation. | PNO.D1 | Sequencer |
| U_LEAD_POS_OFS_PNO_POS | V | Offline | Voltage offset of POS current lead measured during PNO POS | PNO.A1 | PMA |

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|---|---|---|---|---|---|
| U_LEAD_NEG_OFS_PNO_POS | V | Offline | Voltage offset of NEG current lead measured during PNO POS | PNO.A1 | PMA |
| U_LEAD_POS_OFS_PNO_NEG | V | Offline | Voltage offset of POS current lead measured during PNO NEG | PNO.A1 | PMA |
| U_LEAD_NEG_OFS_PNO_NEG | V | Offline | Voltage offset of NEG current lead measured during PNO NEG | PNO.A1 | PMA |
| U_LEAD_POS_ PNO_POS | V | Offline | Max voltage of POS current lead during POS cycle measured during offline analysis | PNO.A1 | PMA |
| U_LEAD_NEG_ PNO_POS | V | Offline | Max voltage of NEG current lead during POS cycle measured during offline analysis | PNO.A1 | PMA |
| U_LEAD_POS_ PNO_NEG | V | Offline | Max voltage of POS current lead during NEG cycle measured during offline analysis | PNO.A1 | PMA |
| U_LEAD_NEG_ PNO_NEG | V | Offline | Max voltage of NEG current lead during NEG cycle measured during offline analysis | PNO.A1 | PMA |
| R_LEAD_POS_PNO_POS | Ohm | Offline | Max POS lead resistance calculated during PNO POS offline analysis | PNO.A1 | PMA |
| R_LEAD_NEG_PNO_POS | Ohm | Offline | Max NEG lead resistance calculated during PNO POS offline analysis | PNO.A1 | PMA |
| R_LEAD_POS_PNO_NEG | Ohm | Offline | Max POS lead resistance calculated during PNO NEG offline analysis | PNO.A1 | PMA |
| R_LEAD_NEG_PNO_NEG | Ohm | Offline | Max NEG lead resistance calculated during PNO NEG offline analysis | PNO.A1 | PMA |
| L_CIRCUIT_PNO_POS | H | Offline | Load inductance calculated during PNO POS offline analysis | PNO.A1 | PMA |
| L_CIRCUIT_PNO_NEG | H | Offline | Load inductance calculated during PNO NEG offline analysis | PNO.A1 | PMA |
| DRDT_POS_PNO_POS | Ohm/s | Offline | Rate of change of POS lead resistance with time at PNO POS current | PNO.A1 | PMA |
| DRDT_NEG_PNO_POS | Ohm/s | Offline | Rate of change of NEG lead resistance with time at PNO POS current | PNO.A1 | PMA |
| DRDT_POS_PNO_NEG | Ohm/s | Offline | Rate of change of POS lead resistance with time at PNO NEG current | PNO.A1 | PMA |
| DRDT_NEG_PNO_NEG | Ohm/s | Offline | Rate of change of NEG lead resistance with time at PNO NEG current | PNO.A1 | PMA |

| | | | | | |
|---|---|---|---|---|---|
| R_MAGNET_PNO_POS | Ohm | Offline | Magnet resistance calculated during PNO POS offline analysis. | PNO.A1 | PMA |
| R_MAGNET_PNO_NEG | Ohm | Offline | Magnet resistance calculated during PNO NEG offline analysis. | PNO.A1 | PMA |
| U_PC_OFS_PNO_POS | V | Offline | Average PC offset voltage when at zero current calculated during PNO POS offline analysis | PNO.A1 | PMA |
| U_PC_OFS_PNO_NEG | V | Offline | Average PC offset voltage when at zero current calculated during PNO NEG offline analysis | PNO.A1 | PMA |
| I_COMMISSIONED | A | Offline | Equals I_PNO after successful commissioning of the test sequence | HCA PCR Circuit Release d | MP3 |