Digitizer Status Update & SDR System & Integration Options

https://edms.cern.ch/document/1823376

R. J. Steinhagen

with input from: R. Bär, C. Handel, J. Fitzek, D. Ondreka, V. Sanjari, A. Schwinn

Scope

- FAIR and notably the FAIR Control Centre will deploy a ‘fully-digitial’ control paradigm:
  - automatic monitoring
    - performance tracking & early fault detection
    - quantitative/semi-automatic feedback and setup applications
  - assisted isolation of HW faults (‘ref-actual’-monitoring)
  - remote expert diagnostics (as needed)
  - also: pre-requisite prior to major ‘alt-HKR’ upgrades and/or move of operations to FCC

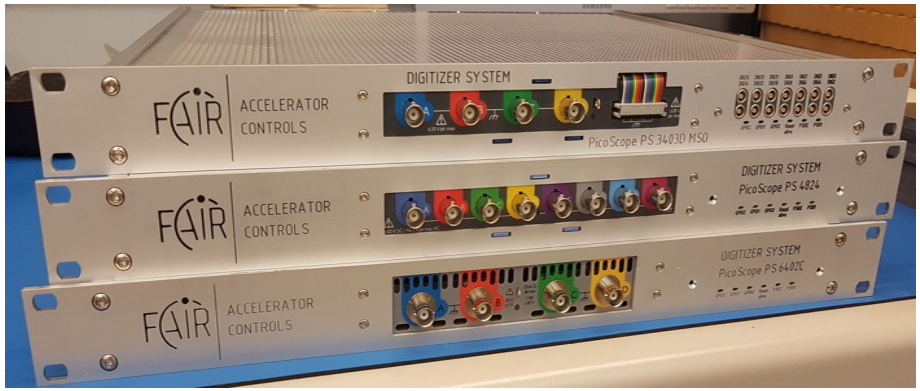
- Primary goals
  - generic abstraction of the vendor-specific digitizer software interfaces
    - explicitly open for new/future vendor/digitizer models extensions
  - limited range of generic user-definable data post-processing on the acquired data
  - control system integration by providing standardised FESA interface

ongoing..

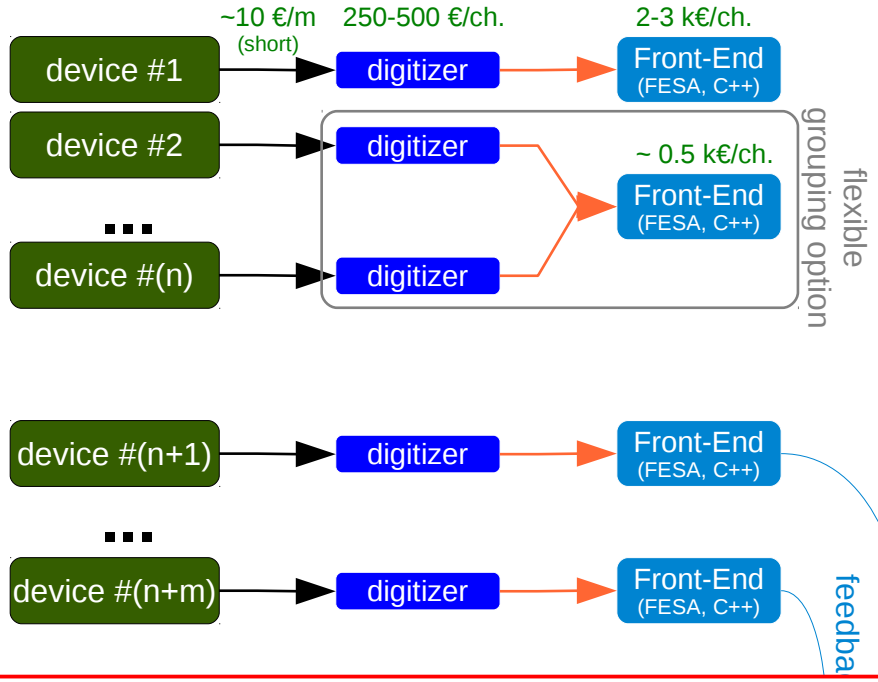
- Secondary goals
  - simplify further extensions, compactness, readability, re-usability, testability, and maintainability of the FESA implementation
  - Use of open-source signal processing and data fitting libraries
    - GNU-Radio – frame-work: https://www.gnuradio.org
    - ROOT – frame-work: https://root.cern.ch

- Not a new concept, existing specifications:
  - “Soft Oscilloscope System” https://edms.cern.ch/document/1176042/3
  - “Digitization of Analog Signals in the FAIR Accelerator Complex” https://edms.cern.ch/document/1823376/

Digitization of Analog Signals at FAIR I/II
https://edms.cern.ch/document/1823376/



- targeted concept
  (underlying assumption: scopes/digitizers are cheap, RF switches are expensive)



start deployment ≥2018 (SIS18), crucial for:
- migration to new FAIR Control Centre (FCC),
- optimisation of commissioning & operation
- tracking/isolation of faults (↔ post-mortem)
- less-biased performance indicator

link: more details

Digitization of Analog Signals at FAIR II/II

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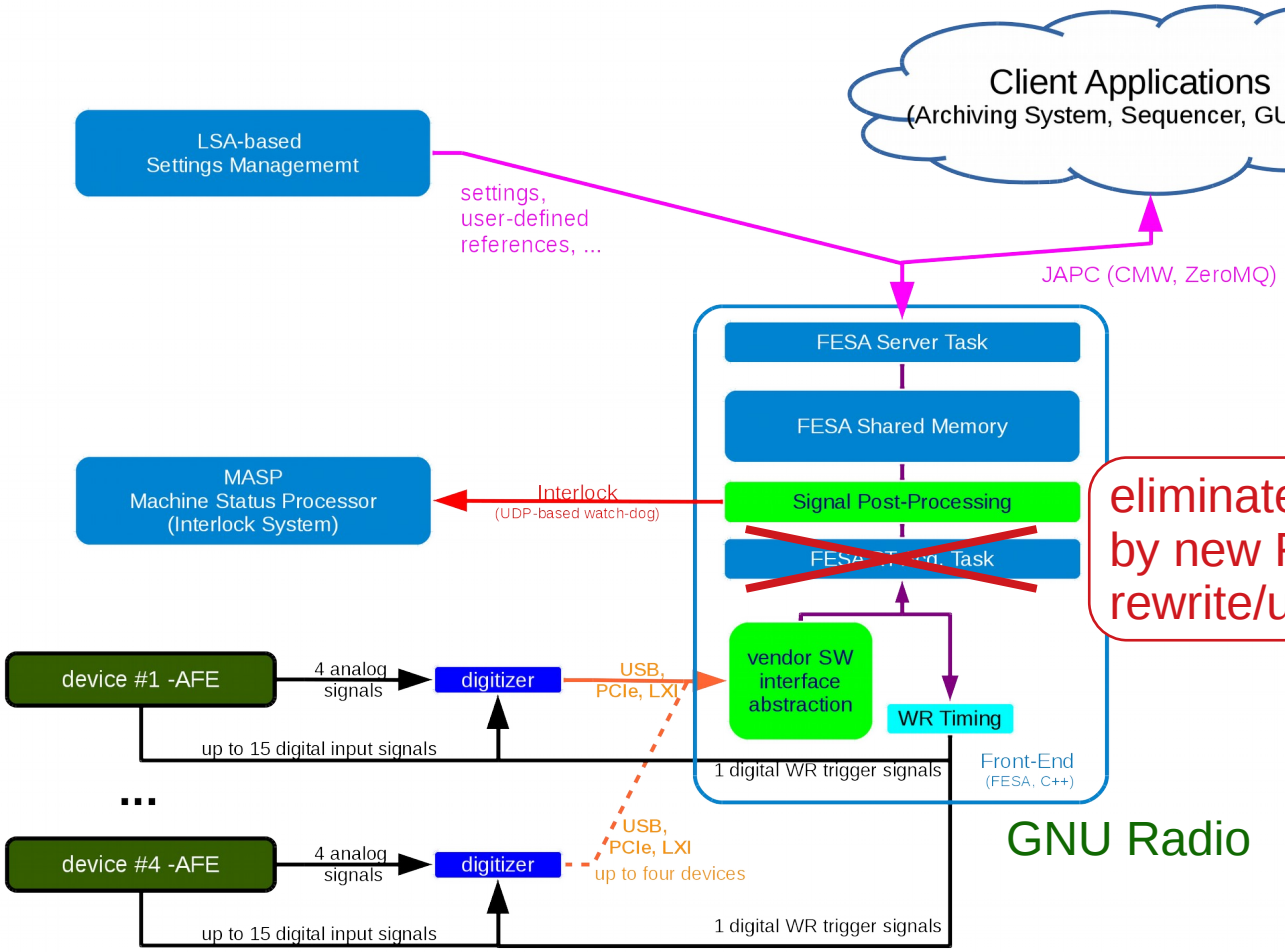

eliminated/simplified by new FESA rewrite/upgrade

Quality Management	Document Type:	Document Number: F-CS-C-02e	Date: 2017-06-27
FAIR	Common Specification	Template Number: Q-FO-QM-0005	Page 1 of 30

Document Title:	On the Digitization of (generic) Analog Signals in the FAIR Accelerator Complex
Description:	Detailed specification for the integration of time-domain digitizers with analog bandwidths and sampling frequencies ranging from DC to up to hundreds of MHz into the accelerator control system
Division/Organization:	FAIR
Field of application:	FAIR Project, existing GSI accelerator facility
Version	V 0.4

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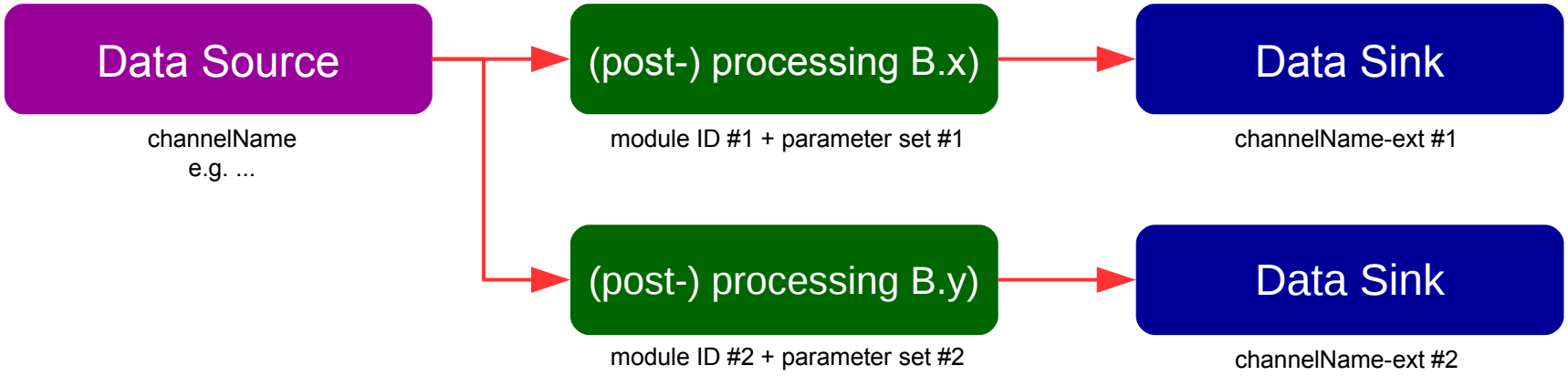
F-CS-C-0002e_Digitisation_of_Analog_Signals_v1.0.odt — Hardcopy will not be controlled

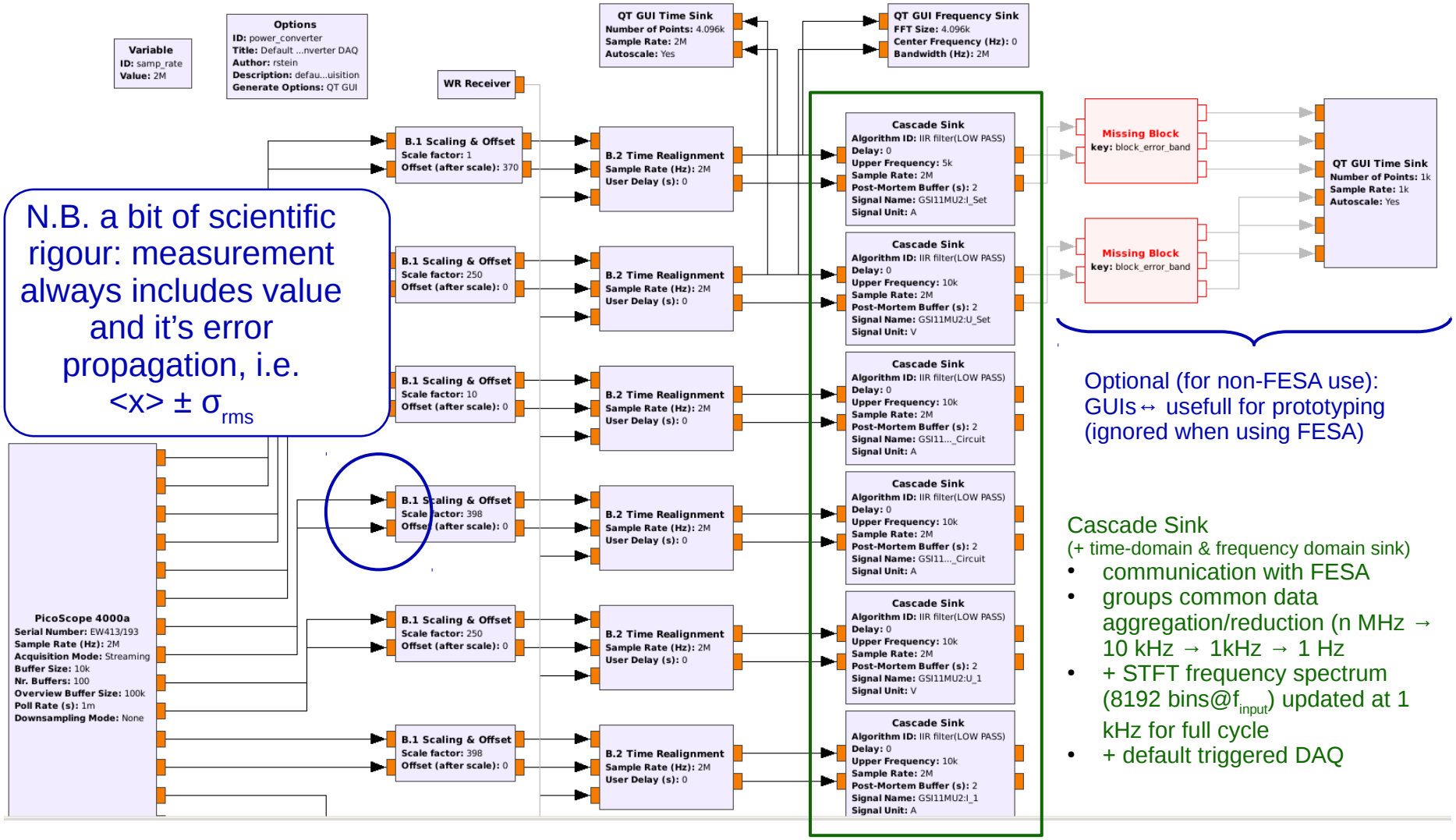
General Signal-Flow Scheme

N.B. GNU-Radio real-time streaming processing inspired



- Scheme can be further cascaded and combined with other modules
  - based on GNURadio‘s signal-flow concept https://www.gnuradio.org/
    - N.B. there are conceptually also other similar other projects: e.g. ADS, QUCS, Spice, LabVIEW … but with a different non-real-time (RF) signal processing

General Signal-Flow Scheme
Simple Example – AEG Dipole Acquisition



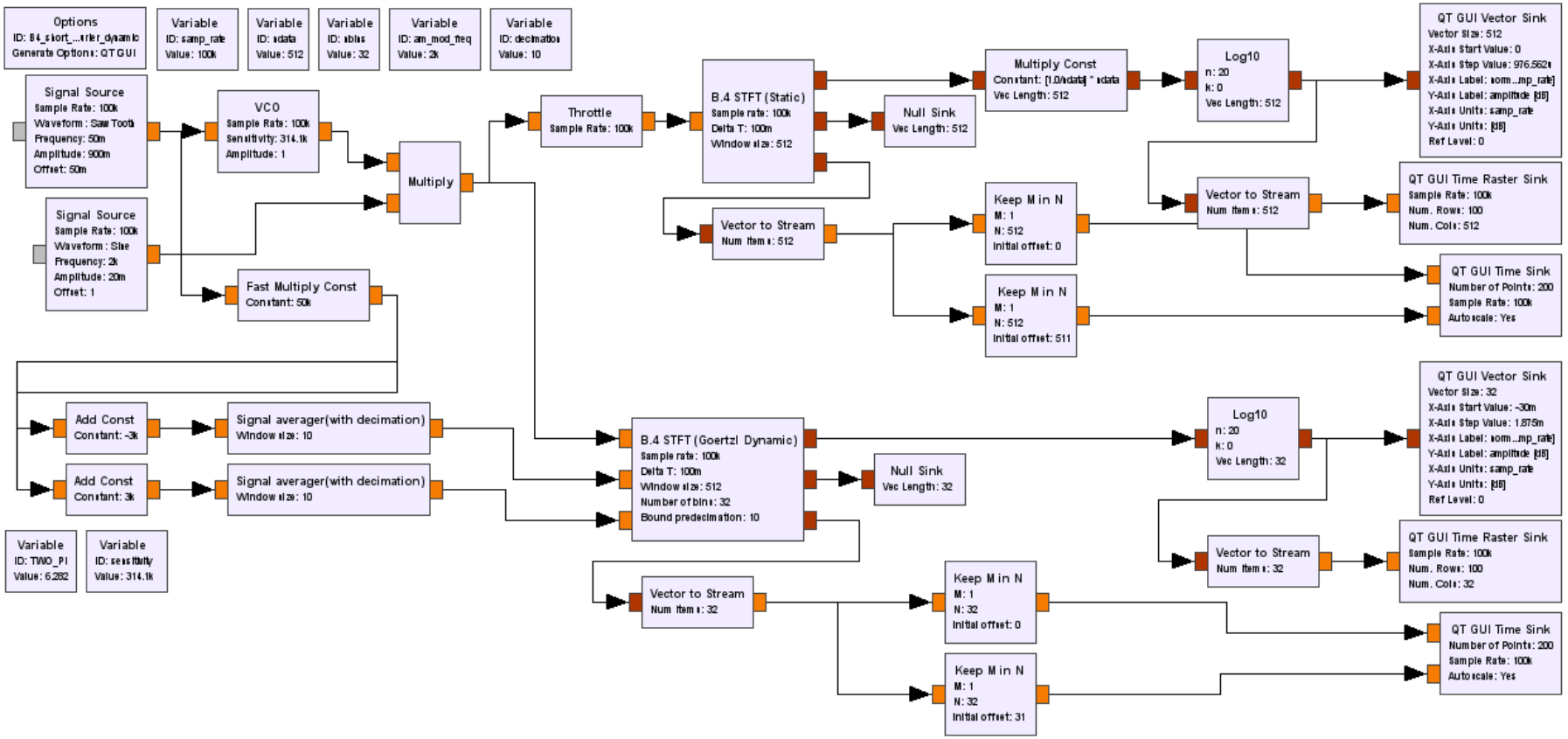
N.B. a bit of scientific rigour: measurement always includes value and it's error propagation, i.e. $\langle x \rangle \pm \sigma_{rms}$

Optional (for non-FESA use): GUIs ↔ usefull for prototyping (ignored when using FESA)

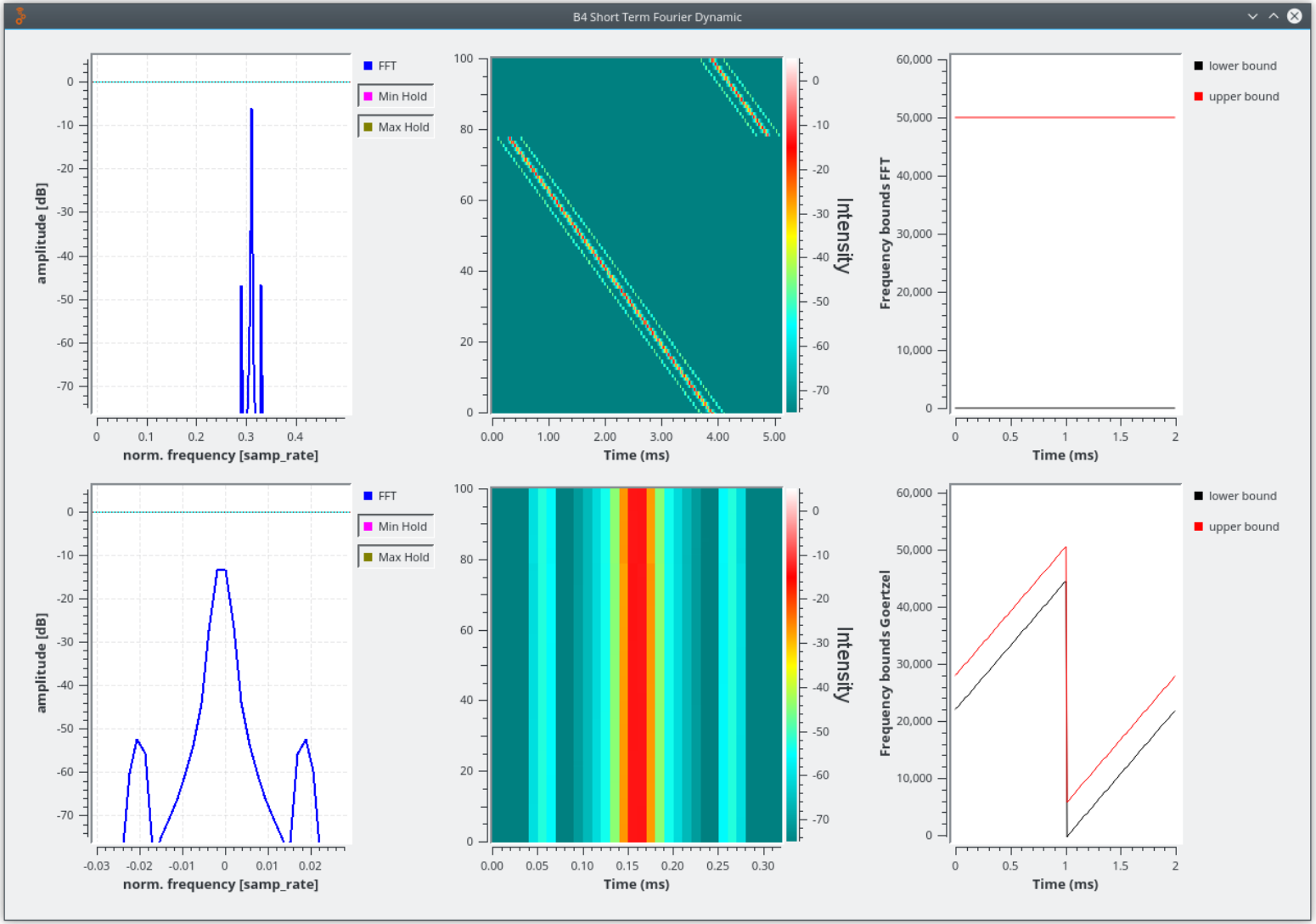
Cascade Sink
(+ time-domain & frequency domain sink)

- communication with FESA
- groups common data aggregation/reduction (n MHz → 10 kHz → 1kHz → 1 Hz
- + STFT frequency spectrum (8192 bins@f_{input}) updated at 1 kHz for full cycle
- + default triggered DAQ

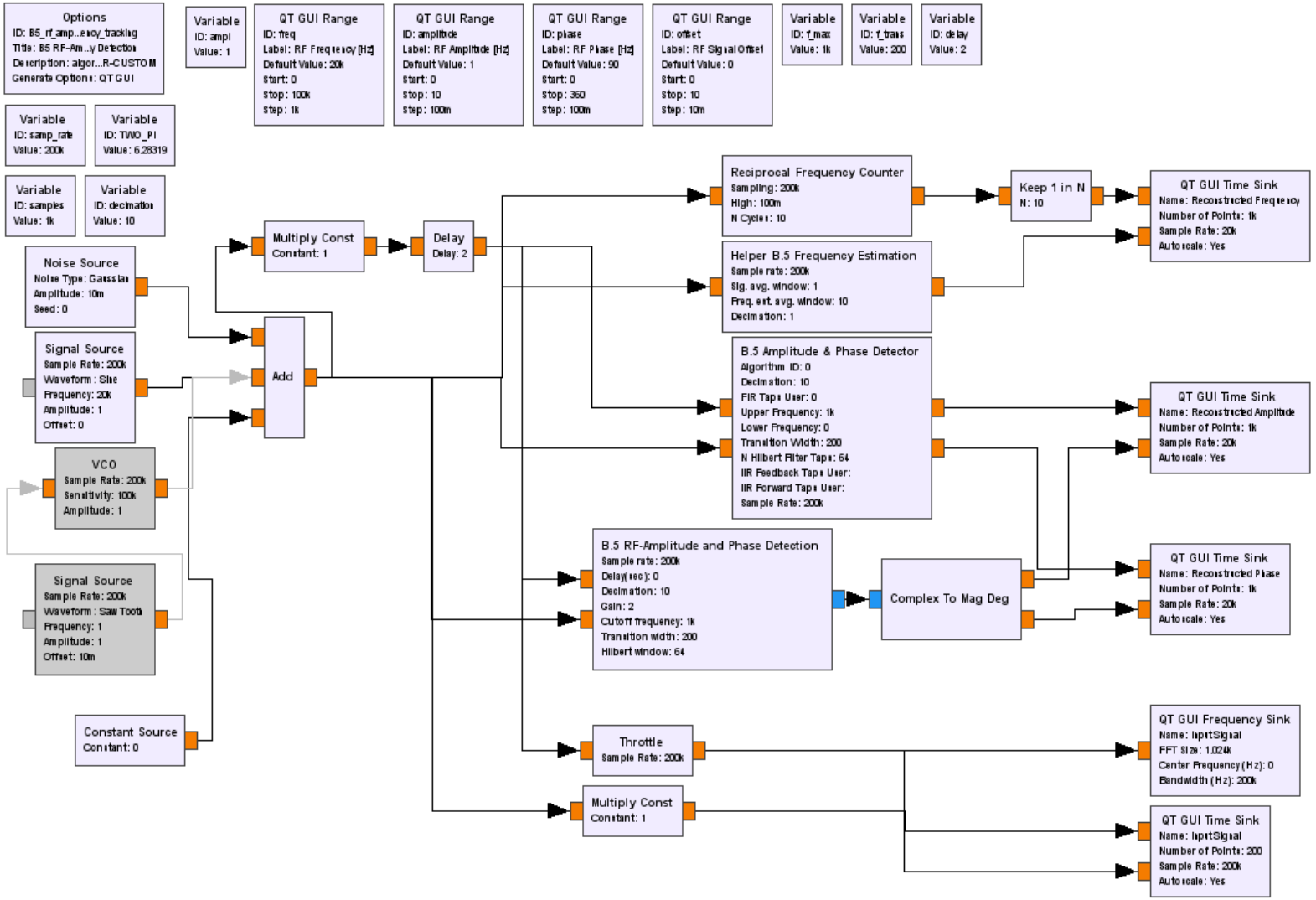
Short-Term-FFT, Goertzel-Transform etc. Example I/II



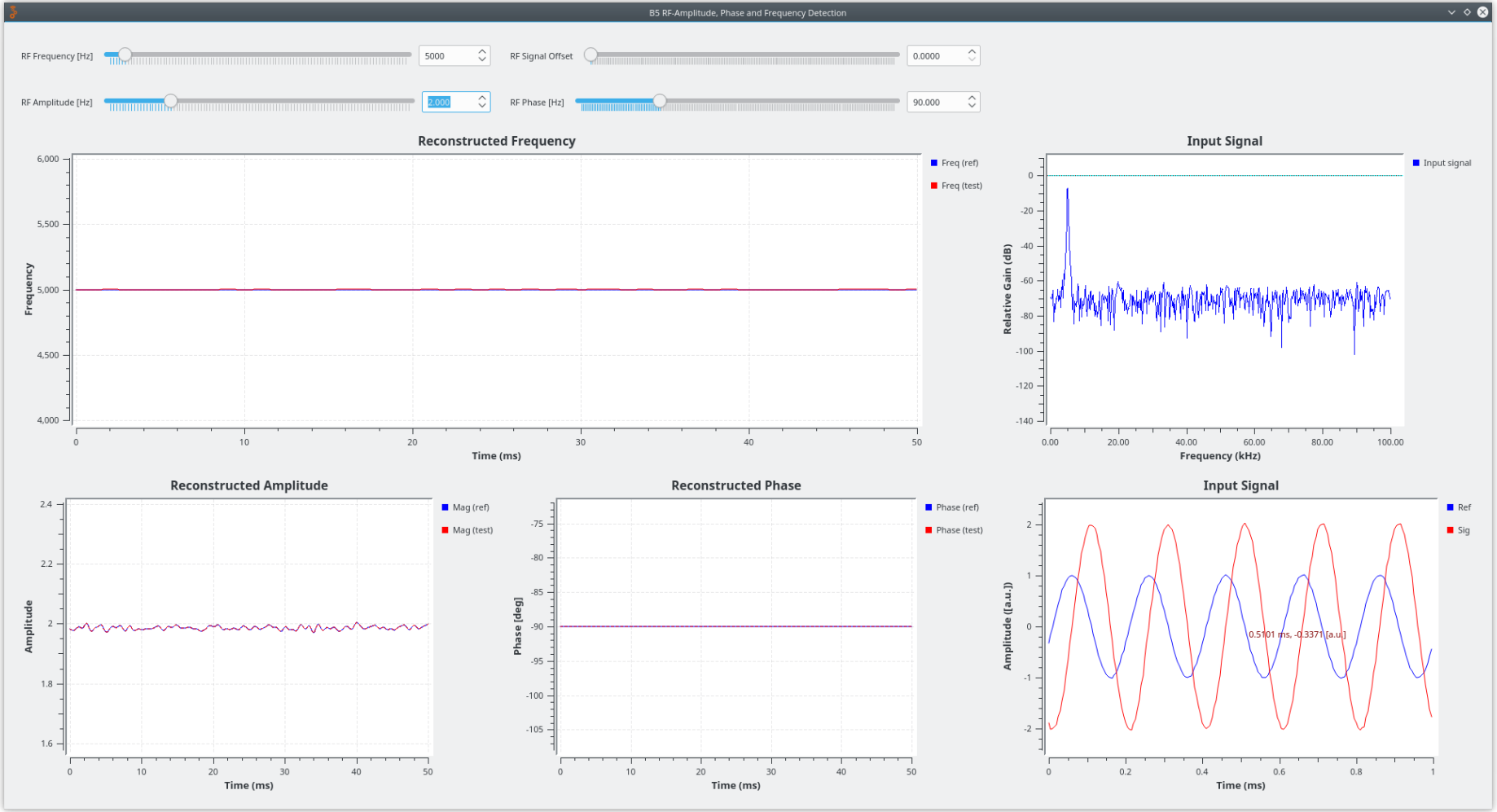
Short-Term-FFT, Goertzel-Transform etc. Example II/II



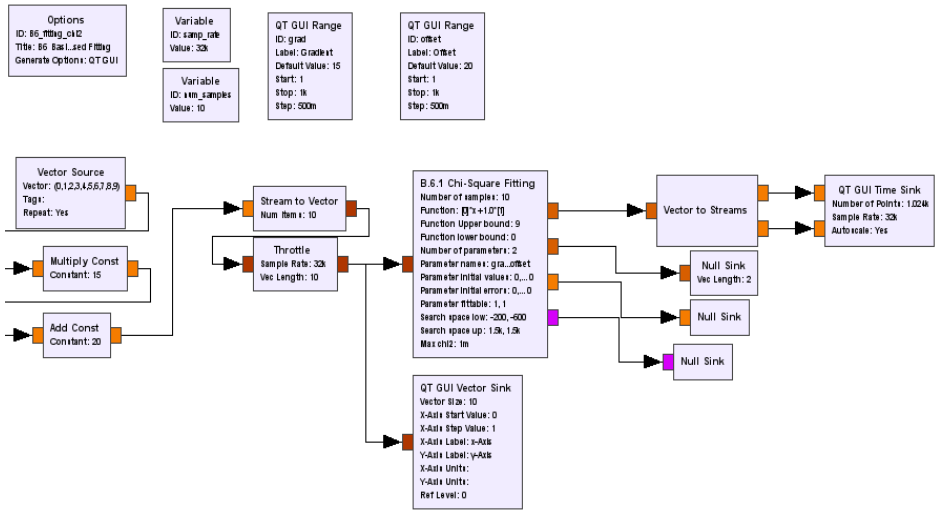
RF-Amplitude, Phase, and Frequency Detection Example I/II

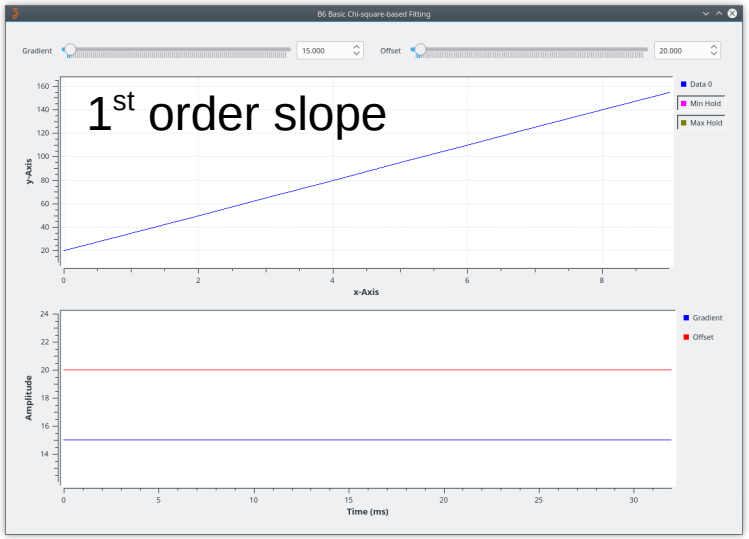


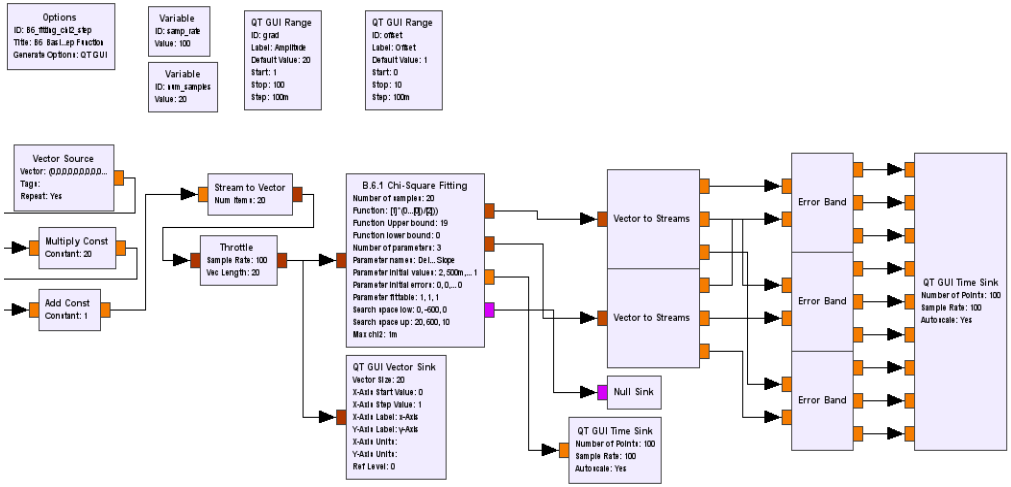
RF-Amplitude, Phase, and Frequency Detection Example II/II

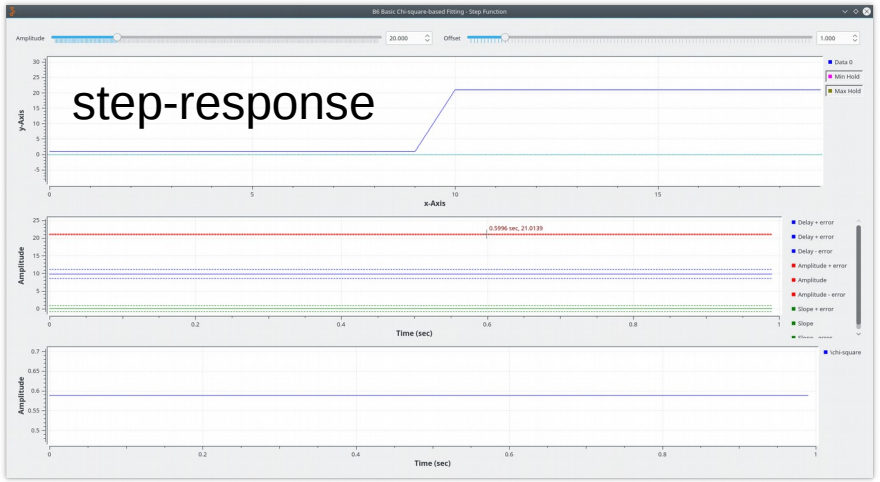


Generic Chi-square based fitting Example



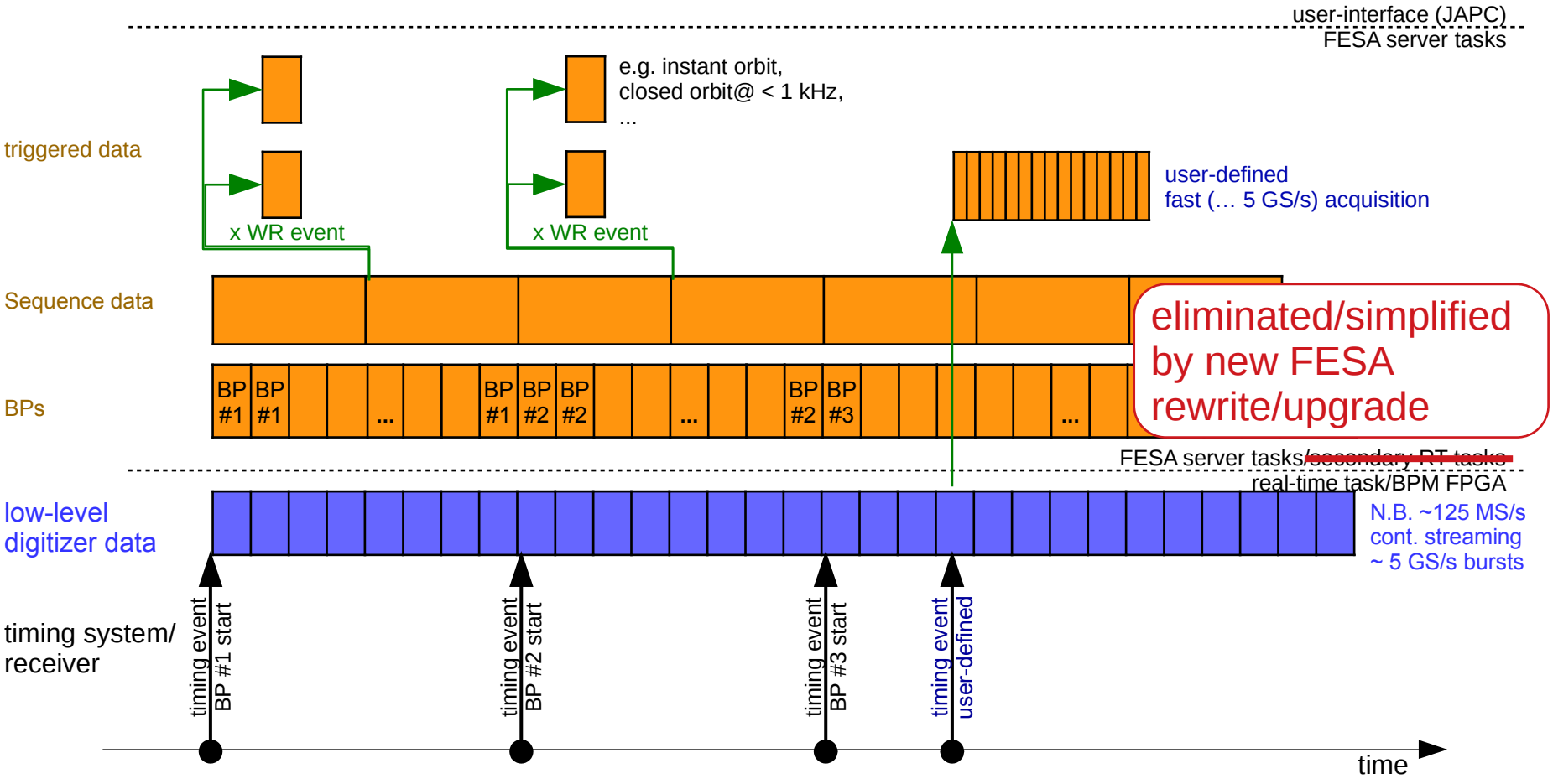






Low-Level Acquisition Modes
A.1) Streaming-mode acquisition I/II

acquisition schematic:



Generic Acquisitions I/II
Specified FESA Data Streams

Following modes of acquisition would be expected to be served simultaneously (though some of them could be implemented as down-sampled copies of the higher bandwidth acquisition):

A. Slow-acquisition (FESA property: 'Acquisition') – sub-choices (selected via CMW-filter):

1) **'Sequence'** acquisition between 'beam injection' and 'beam extraction': the specific signal averaged and decimated to the rate needed for the given client (e.g. 1 kHz).
   → *property notifies complete trace as a function of time at the end of the sequence (up to 30-60 s)*
2) **'Continuous'** real-time data publication during the cycle (↔N.B long SIS100 cycles and/or storage rings):
   → *property notifies single measurement at typical update rate around 10-25 Hz*
   - use-case: user-level applications (inj./extr. steering), software-based real-time feedbacks, ...
3) **'Instant'** signal acquisition: → *property notifies single measurement at pre-defined time delays (ms-scale)*
   - software interlock on injection/extraction orbit deviations (via MASP)

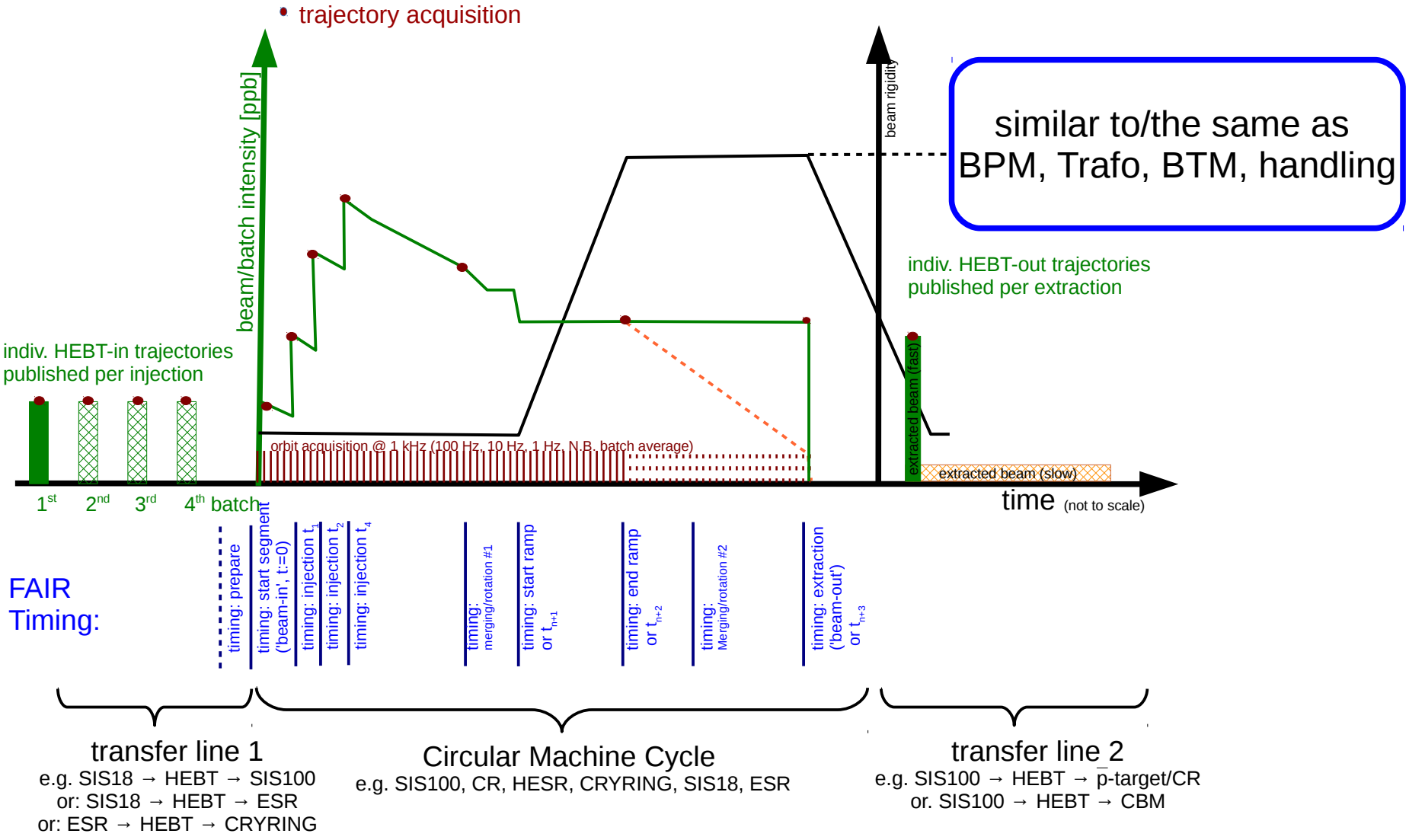
B. Fast block-mode acquisition (also 'Acquisition'):

- up to 10 external user-defined timing triggers per sequence (ie. each injection, extraction etc.)
  - corresponding CMW property subscription: e.g. 'TRIGGERED' or name of specific timing event
- horizontal channel settings are assumed to be fixed per digitizer

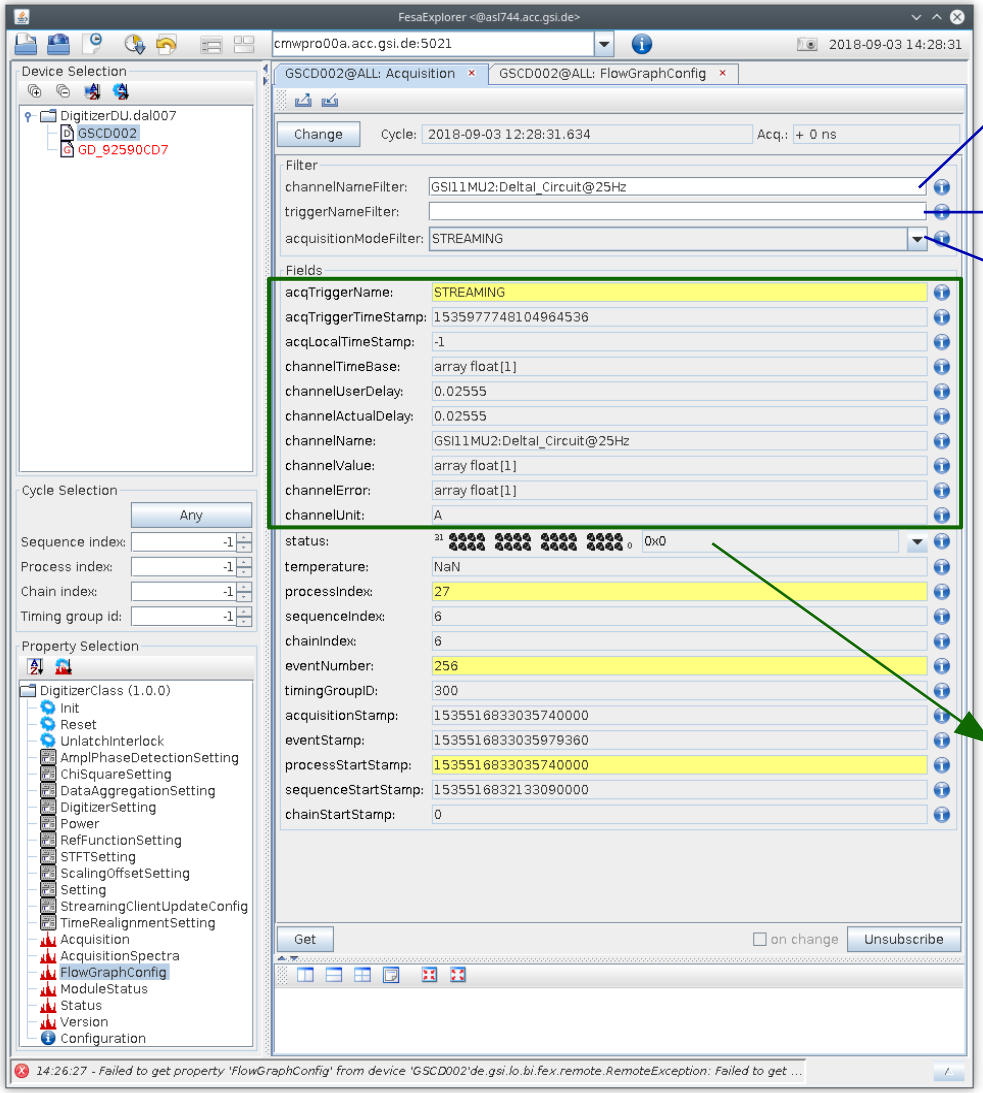
C. Post-Mortem (FESA property 'PostMortem'): not finalized but provisionally:

1) first circular buffer storing each signals @ 1 kHz for the last second of beam or full cycle
2) second circular buffer storing the last 1k (10k?) turns at maximum sampling rate

Data Acquisition, Client Interfaces & Synchronisation



FESA Acquisition(Sepctra) Property Layout



signal name, e.g. '*GSI11MU2:I_Circuit@1kHz*'

WR event (optional), e.g. '*CMD_BEAM_INJECTION*', '*CMD_BEAM_EXTRACTION*', '*CMD_START_ENERGY_RAMP*', '*CMD_CUSTOM_DIAG_[1,3]*'

acquisition mode:
- STREAMING
- FULL SEQUENCE
- SNAPSHOT
- POST_MORTEM
- TRIGGERED

user data:
- acqTriggerStamp (UTC-seconds of trigger/start)
- channelTimeBase (N.B. time stamps relative w.r.t. 1st injection)
- channel[Actual/User]Delay (↔ bunch-to-bucket-inj./group delay)
- channelName
- channelValue (N.B. array)
- channelError (N.B. array)
- channelUnit
- [..]

GUI in preparation

Digitisation of Analog Signals
Next Steps

- Sub-categories:
  - a) time-domain: functional actual-vs-reference monitoring (DC – up to 2GHz)
  - b) frequency-domain: SA- & VNA-type funct. $\Delta f_{bw} \approx 20$ MHz@fLO≈DC…6 GHz
  - c) video-signal (IPM, screens, etc.) → not covered
    - existing BI technology/integration, main issue: budget/MC commitment
    - need interim solution for 'alt-HKR' retrofitting → personell resources needed
  - d) generic signals < 1 MHz bandwidth → also not covered (e.g. QPS, BI)
    - different strategy: local low-cost high-ADC-density controller, ...

✓ < 30 MHz ↔ time-domain digitizer
> 30 MHz → proper SDR ✓

- Frequency-domain covering Software-Defined-Radio (SDR)-like functionalities:
  - e.g. RF vector signal analyzer, RF network analyzer, RF signal generator, ...
    - DAQ of Rx-path is very similar to existing time-domain digitizers
      - N.B. often already existing GNU Radio integration + (tbd.) integration of White-Rabbit-Trigger/Synchronisation integration
    - Open-question:

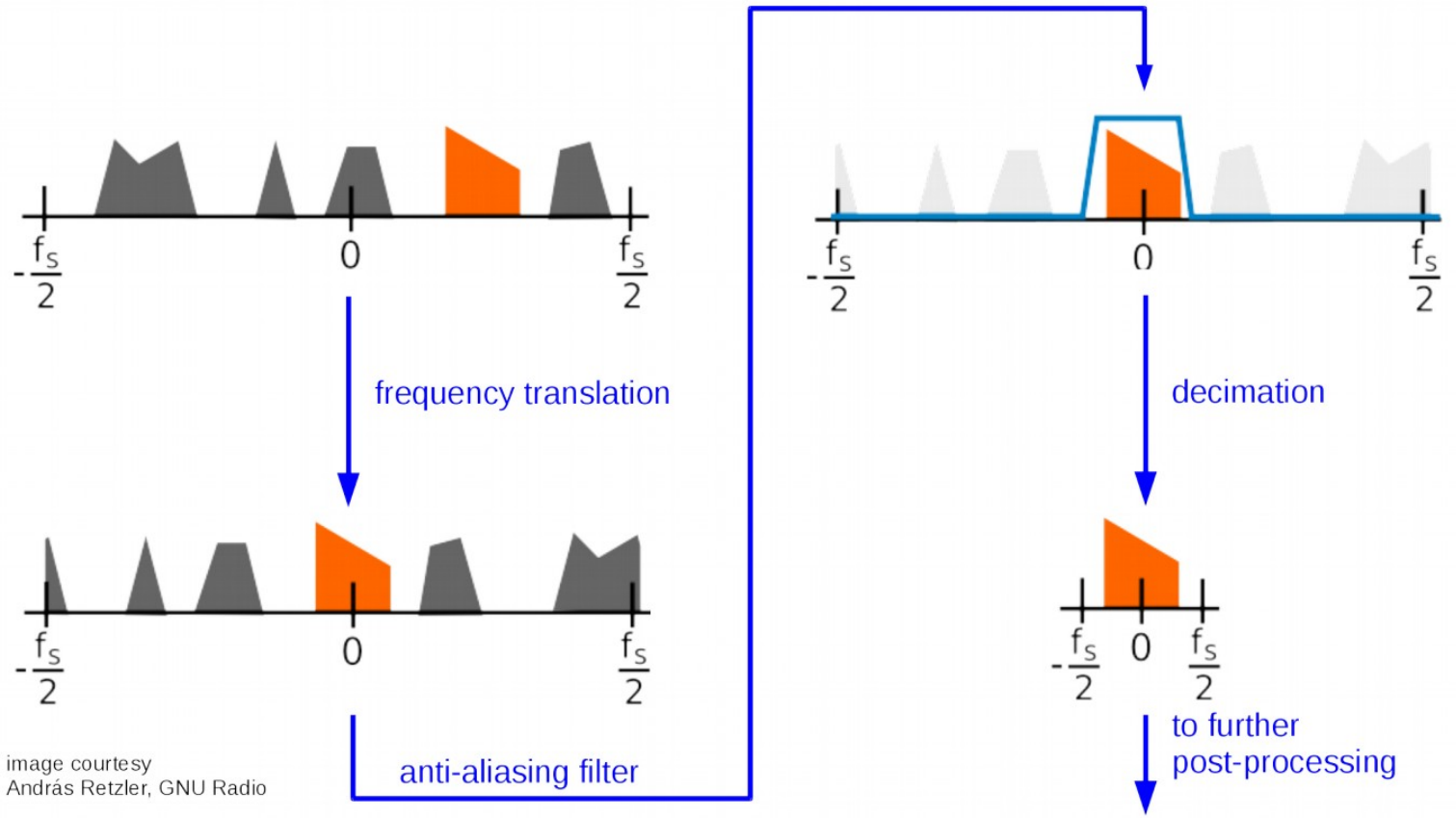
      A) SDR hardware choice (next slide)

      B) Integration of Tx-path: signal/function types, triggering schemes

      C) Low-level RF feedback functionalities
        - probably requires (custom) FPGA modifications (functionality needed)

Software Defined Radio

Wikipedia: “[..] components that have been traditionally implemented in hardware (e.g. mixers, filters, amplifiers, modulators/demodulators, detectors, etc.) are instead implemented by means of software on a personal computer or embedded system. [..]”



Software-defined Radio
Hardware choices – Impressions

- wide range of academic, commercial, and military applications:
  - cellular radios (3G, 4G, 5G), (passive) radar systems, SIGINT, …
  - market at its infancy and will likely continue to grow significantly
- focused on commercial/open-source systems → easier integration (GNU Radio, less NDAs, …)

Software-defined Radio
Market Survey & Pre-Selection

	RTL-SDR	HackRF One	BladeRF x40	BladeRF x115	Ettus N210 (basic RF)	Ettus B210	LimeSDR	Ettus X310 (UBX 40/160)	Crimson TNG
Frequency Range	22MHz-2.2GHz	1MHz-6GHz	(50 kHz) 300MHz-3.8GHz	(50 kHz) 300MHz-3.8GHz	1MHz-250MHz	70MHz-6GHz	100kHz-3.8GHz	10MHz-6GHz	100kHz-6GHz
RF Bandwidth	3.2MHz	20MHz	(28) 40MHz	(28) 40MHz		61.44MHz	61.44MHz	40 (160)MHz	>1200 MHz
Sample Depth [bits]	8 bits	8 bits	12 bits	12 bits	14 bits	12 bits	12 bits	14 bits	
Sample Rate [MS/s]	3.2	20	40	40	50	61.44	61.44	200	> 200
Transmitter Channels	0	1	1	1	2	2	2	2	4
Receivers	1	1	1	1	2	2	2	2	2
DDC/DUC res. [mHz]					25				
Duplex	N/A	Half	Full	Full	Full	Full	Full	Full	Full
Interface	USB 2.0	USB 2.0	USB 3.0	USB 3.0	Gigabit-Ethernet	USB 3.0	USB 3.0/ PCIe x4	2 x 10 Gigabit/ PCIe x4	20 Gigabit
FPGA			Altera 40KLE Cyclone IV	Altera 115KLE Cyclone IV	Xilinx Spartan 3A-DSP 3400	Xilinx Spartan 6 XC6SLX150	Altera EP4CE40F23 Cyclone IV	Xilinx Kintex-7	Altera Arria V ST 5ASTMD3E3F31
Programmable Logic Gates	N/A	64 macrocell CPLD	40k	115k	53k	100k	40k	406k	a lot
RF/ADC Chipset	RTL2832U	MAX5864, MAX2837, RFFC5072	LMS6002M	LMS6002D	custom & AD9777	AD9361	LMS7002M	custom & ADS62P48	ADF4355
Open Source	No	Full	Schematic, Firmware	Schematic, Firmware	Schematic, Firmware	Schematic, Firmware	Full	Schematic, Firmware	Schematic, Firmware
Oscillator Precision	?	+/-20ppm	+/-1ppm	+/-1ppm	+/-2.5ppm	+/-2ppm	+/-1ppm initial, +/-4ppm stable	+/-2.5ppm	+/-2.5ppb
Transmit Power	N/A	-10dBm+ (15dBm @ 2.4GHz)	6dBm	6dBm	10dBm+	10dBm+	~10dBm	10dBm+	10dBm+
SW interface	GNU Radio	GNU Radio	GNU Radio	GNU Radio	GNU Radio	GNU Radio	GNU Radio	GNU Radio	GNU Radio
Approx. Price	~$10	$299	558 €	750 €	2222 €	1220 €	249 €	7660 €	17917 €
Approx. Price (PCIe)							666 €	8435 €	> 50 kEUR

N.B. 61.44 MS/s ↔ USB 3.0 limit
50 MS/S ↔ 1 Gigabit link

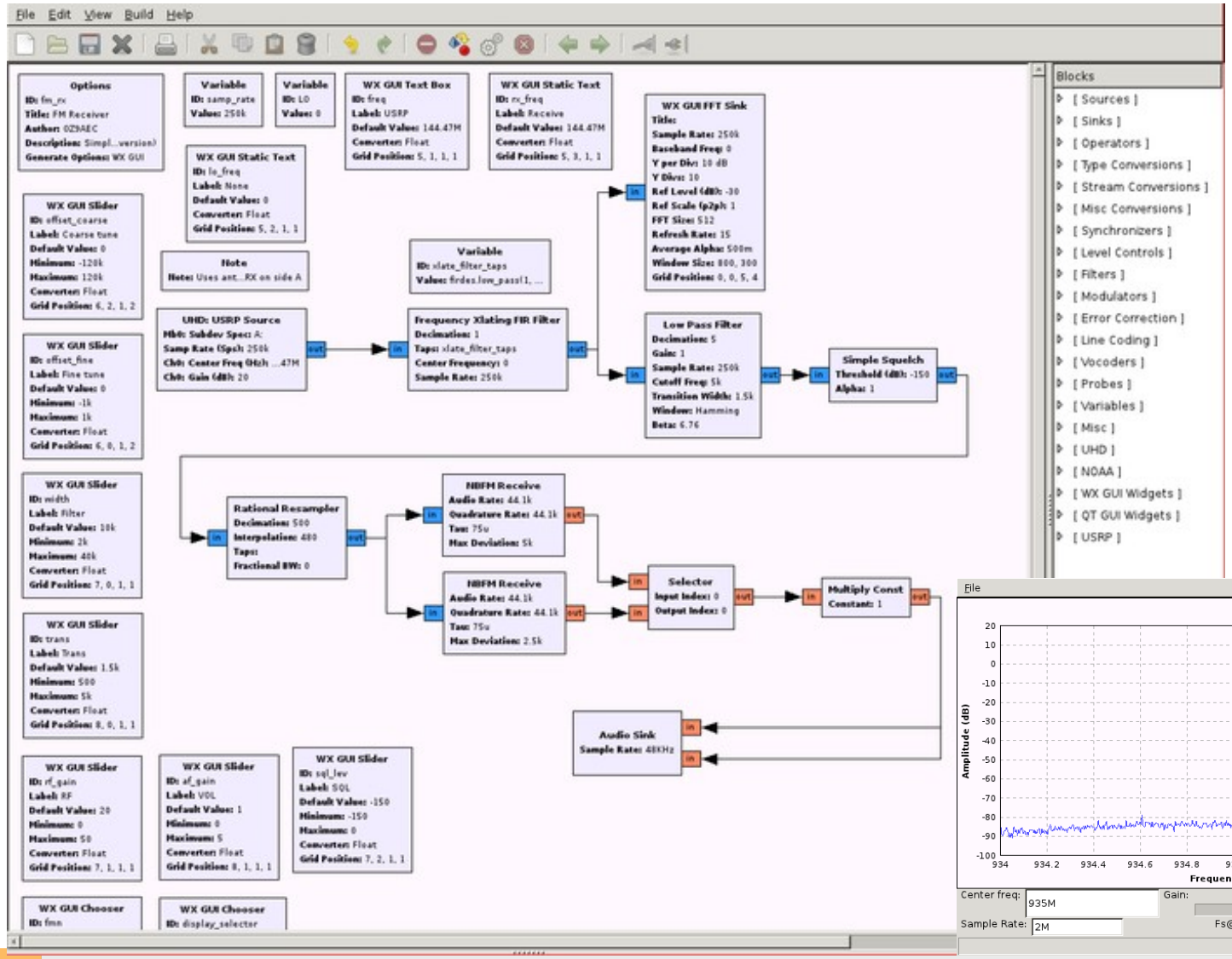
low-end

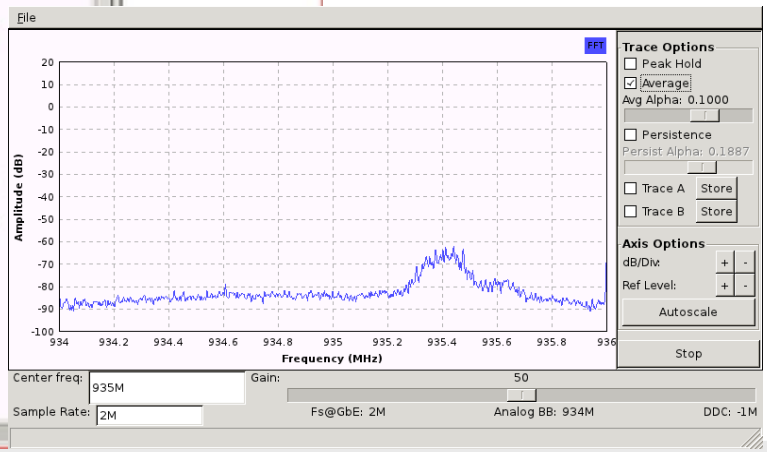
high-end

Most SDRs already integrated in GNU-Radio (via UHD)

N.B. still requires WR event/synchronisation (via GPIO? Rx?)

here:
simple FM receiver





Known/possible SDR Applications@FAIR

- SIS18/SIS100 K.O. exciter monitoring/signal generation:
  - broad-band signal surveillance (+ time-domain digitizer)
  - flexible spectrum & time dependencies for excitation
  - option: fast(er) spill-extraction FB?

- Generic accelerator-related diagnostics
  - Long. Schottky: momentum width, energy mismatch, intensity, ...
  - trans. Schottky: Q/Q', emittances, … ??
  - experiments: use-cases see V. Sanjari's presentation

- RF leakage monitoring/EMC compliance for UNILAC RF driver (pLinac?) ??
  - N.B. 36.136 MHz ↔ (civ/mil: BOS, micros, ...)
  - N.B. 108.408 MHz ↔(civ/mil: aviation, navigation, ...)

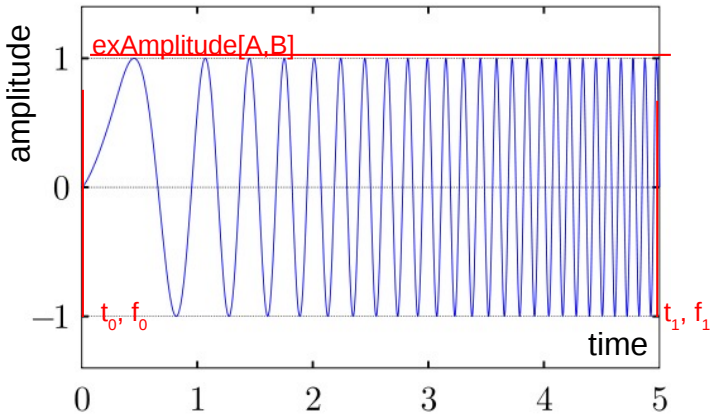
- Low-Level RF (reuse same HW/SW platform)?
  - second-/third-order harmonic measurements

- <you application here> – it's a generic CO platform that can be further expanded:
  - under the responsibility of CO:
    - Digitizer (SDR) HW integration
    - HW abstraction/driver-integration (GNU Radio)
    - basic signal post-processing & FESA export
  - Under the user responsibility
    - RF analog input adaptation & cabling (ie. AFE, analog front-end)
    - non-standard signal post-processing, i.e. custom FPGA processing/modifications

Integration of Tx-path I/II
– excitation types (+ WR triggered → needs proof-of-concept)

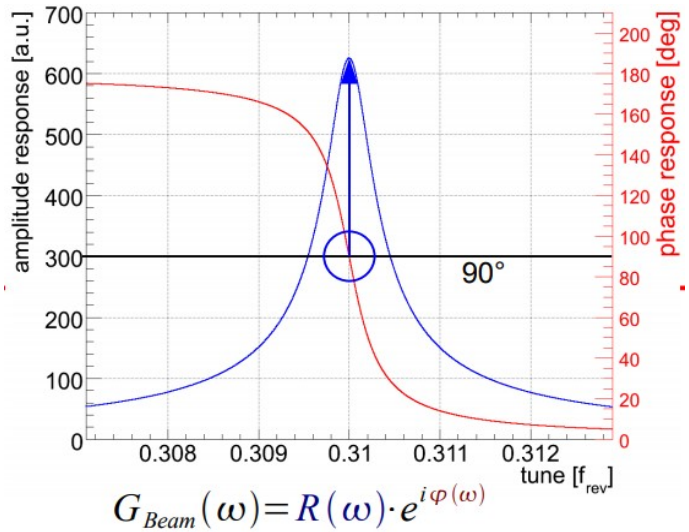
- No excitation/white or remnant noise

- Kick/frequency sweep aka. ‘chirp’
  - enableExcitationTx-[A,B]
  - exAmplitude[A,B]
  - chirpStartDelay t_0, chirpStopDelay t_1
  - chirpStartFreq[A,B] f_0, chirpStopFreq[A,B] f_1
  - + all the above as function of time in cycle/BPC sequence



- Phase-Locked-Loop (PLL) System
  - Similar to chirp but on slower time-scales
  - Beam-Transfer-Function (BTF)

- Bandwidth-limited/shaped white-noise
  - Uniform, Gaussian,Laplacian, Impulse, inverted-Gaussian, ...
  - + all the above as function of time in cycle/BPC sequence



Integration of Tx-path II/II
– excitation types (+ WR triggered → needs proof-of-concept)

- Deterministic signal source
  - sine, square, triangle, saw-tooth, sin(x)/x, gaussian, half-sine
- Arbitrary Waveform Generator (SDR can operate as DDS generator)
  - options are limitless but ressources to implement these are finite → need to prioritise
- External Rx-driven output relation (ie. FB-loop, required FPGA mod)
  - simple PID +simple Smith-Predictor for 1st/2nd-order latency compensation
- Misc:
  - ADC/DAC clockSource = external vs. internal oscillator
  - FirDecimationValue, ...
  - external gating???

Digitizer Status Summary & SDR Open Questions

- FAIR Control Centre (FCC): ‘fully-digitial’ control paradigm
  - pre-requisite prior to ‘alt-HKR’ to FCC move
  - automatic monitoring, performance tracking & early fault detection
  - assisted isolation of HW faults (‘ref-actual’-monitoring) & remote expert diagnostics (as needed)

- Primary goals of digitizer integration:
  1. generic abstraction of the vendor-specific digitizer software interfaces (via GNU Radio)
  2. limited range of generic user-configurable data post-processing on the acquired data
  3. control system integration by providing standardised FESA interfaces

  ✓ ✓ ongoing..

- Sub-categories:
  a) time-domain: functional actual-vs-reference monitoring (DC – up to 2GHz) ✓
  b) frequency-domain: SA- & VNA-type funct. $\Delta f_{bw} \approx 20$ MHz@$f_{LO} \approx$DC…6 GHz
  c) video-signal (IPM, screens, etc.) → not covered (existing BI technology/integration) ✓

  < 30 MHz ↔ time-domain digitizer
  > 30 MHz → proper SDR

- Open-question regarding frequency-domain digitization via Software-Defined-Radios (SDRs):
  1. SDR hardware choice → cross-check favoured candiates
  2. Integration of Tx-path: signal/function types, triggering schemes
     - to be demonstrated: integration of White-Rabbit-Trigger/Synchronisation integration (via GPIO?)
  3. Low-level RF feedback functionalities → … an option to be followed-up?

Appendix

Final Vendor/Model Selection
PicoScopes from Pico Technology

- Low-Bandwidths (< 20 MHz)
  - PicoScope 4824, 7 (8) channels, 11.3 ENOB @ 20 MHz)
    - N.B. ~ 16 ENOB @ 10 kHz ($\Delta I/I_{max} \sim 10^{-5}$)
  - 2018: primarily used for EPC-related systems (→ 2018: “AEG”)
    - planned to digitize: I_{ref}, U_{ref}, I_{actual}, U_{actual}, ΔI, U_{int}, + 1 spare
    - 8th channel for WR timing synchronisation

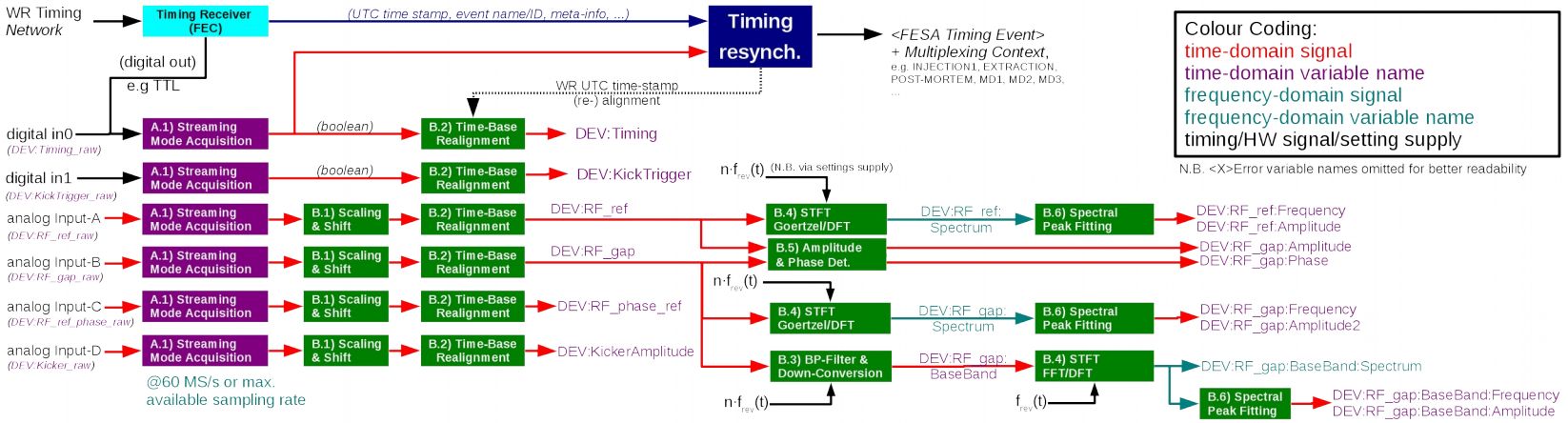
- Medium-range Bandwidths (< 200 MHz)
  - PicoScope 3403D MSO ↔ 3406D MSO), 4 ch, 6.9 ENOB @ 200 MHz
    - N.B. ~ 7.9 (15) ENOB @ 10 MHz (10 kHz) ($\Delta U/U_{max} \sim 10^{-3}$ ($3 \cdot 10^{-5}$))
  - 15 (16) digital channels → triggering e.g. on fast RF loops states, etc.
  - 2018: primarily for Ring-RF (→ “Gap Voltage”) and HV-extraction kicker trigger acquisition

- High-Bandwidth (< 500 MHz, (1 GHz))
  - PicoScope 6402C↔ 6404C, 4 channel, 7.3 (7.9) ENOB @ 500 (200) MHz
  - 2018: primarily used for HV extraction and tune kicker waveform

- Open: specification for further digitizer devices
  - tentatively: Ettus Research SDR for spectra-related applications

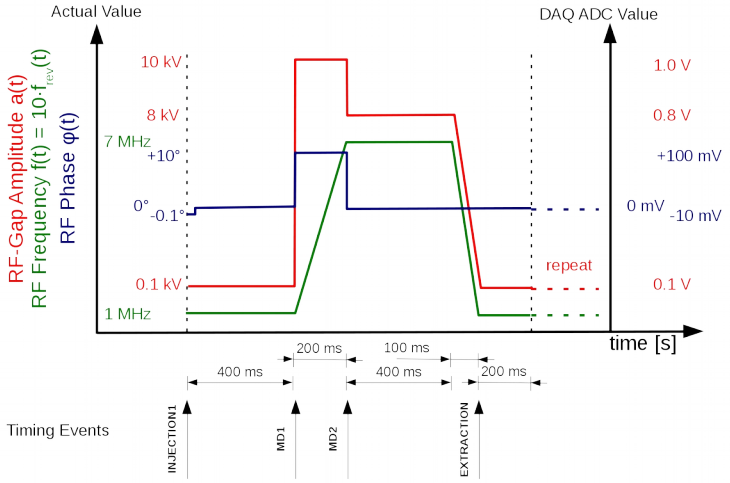
N.B. Ordered/deploy 150+ digitizer for 2018/19 for SIS1/ESR/Cryring

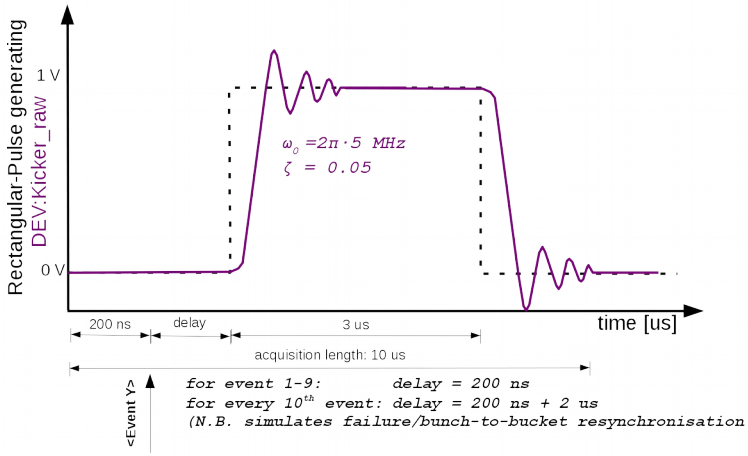
Signal Flow-Graph → SAT I/II



Test Signal Definition:

```
Analog Input-A: DEV:RF_ref_raw (t)    = '1 V'·sin(2π·[f(t) + φ(t)]) + '1% noise'
Analog Input-B: DEV:RF_gap_raw (t)    = a(t)·sin(2π·[f(t) + φ(t)]) + '1% noise'
Analog Input-C: DEV:RF_ref_phase (t)  = φ(t) + '1% noise'
Analog Input-D: DEV:Kicker_raw (t)    = 2nd-orderIIR(Rectangular-Pulse(t-t_event, <parameter see below>), ω_0=2π·5 MHz, ζ= 0.05)+ '2% noise'
```





Signal Flow-Graph → SAT II/II