Common Specification F-CS-C-0002e:

Digitization of (generic) Analog Signals in the FAIR Accelerator Complex – Status & Next Steps –

https://edms.cern.ch/document/1823376

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with input from: R. Bär, C. Handel, J. Fitzek, D. Ondreka

Scope

- FAIR and notably the FAIR Control Centre will deploy a ‘fully-digitial’ control paradigm:
  - automatic monitoring
    - performance tracking & early fault detection
    - quantitative/semi-automatic feedback and setup applications
  - assisted isolation of HW faults (‘ref-actual’-monitoring)
  - remote expert diagnostics (as needed)

- Primary goals
  - generic abstraction of the vendor-specific digitizer software interfaces (explicitly open for new/future vendor/digitizer models extensions)
  - limited range of generic data post-processing on the acquired data
  - control system integration by providing standardised FESA interface

- Secondary goals
  - simplify further extensions, compactness, readability, re-usability, testability, and maintainability of the FESA implementation
  - Use of open-source signal processing and data fitting libraries
    - GNU-Radio – frame-work: https://www.gnuradio.org
    - ROOT – frame-work: https://root.cern.ch

Some notes on: Specifications, Engineering Check & Approval Procedures I/II

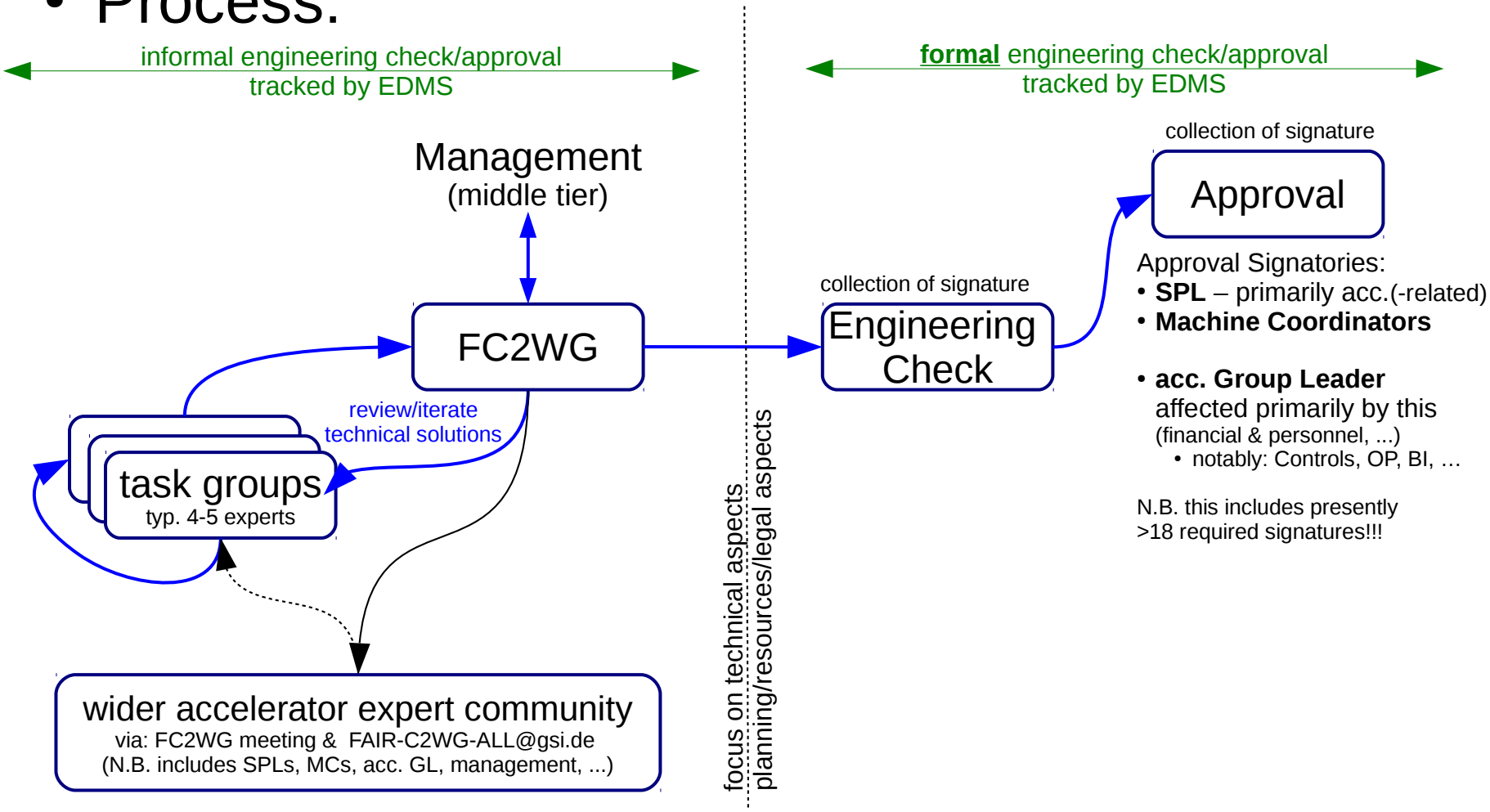
- Common Specification – CS
  - collection of functional user requirements
    - usually facility wide accelerator domain (letter ‘B’), for Digitizer spec domain CO (letter ‘C’)
  - system integration into the facility control and operation concepts
    - primarily reduced to interface description (where necessary)
  - deliberately HW agnostics → view on long-term FAIR base-line
    - keep it open for upgrades, new HW devices or different implementation options

- Detailed Specification – DS
  - specific HW/SW requirements
  - extension of interfaces & requirements not covered by CS
  - handling of additional legal contractual obligations (if not already part of another higher-level specification)
  - FAT/SAT procedures (for ‘in-kind’/external contracts)

- Conceptual Design
  - concrete implementation/interface (usually done by ‘in-kind’ or external partner)
  - extension of interfaces & requirements not covered by DS
  - pre-requisite for the Final Design Review & ‘go-ahead’ for the implementation

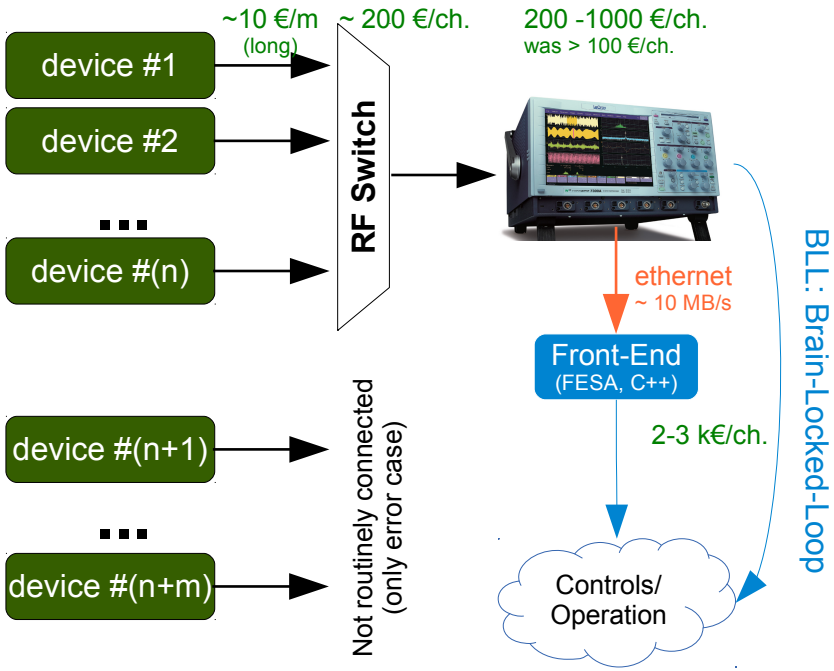
Some notes on: Specifications, Engineering Check & Approval Procedures II/II

- Process:



Main Paradigms

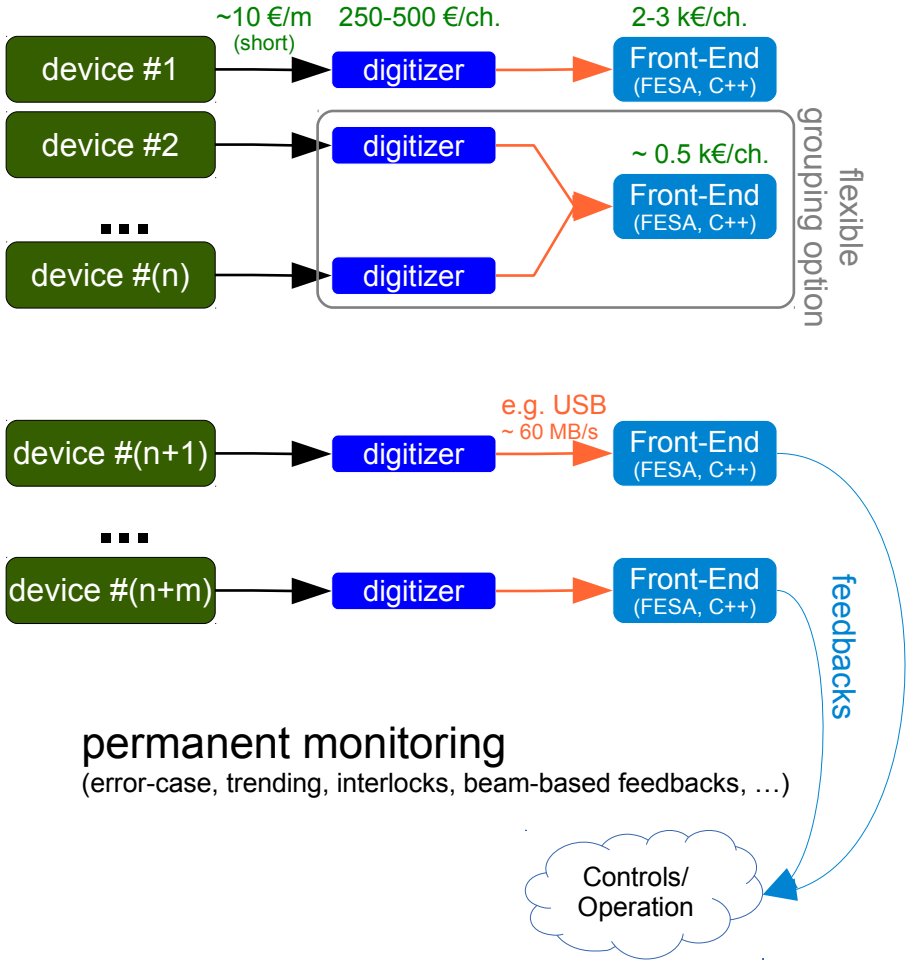
- traditional/old concept
  (underlying assumption: scopes/digitizers are expensive, RF switches are cheap)



on-demand measurement
(selected signals, error-case, …)

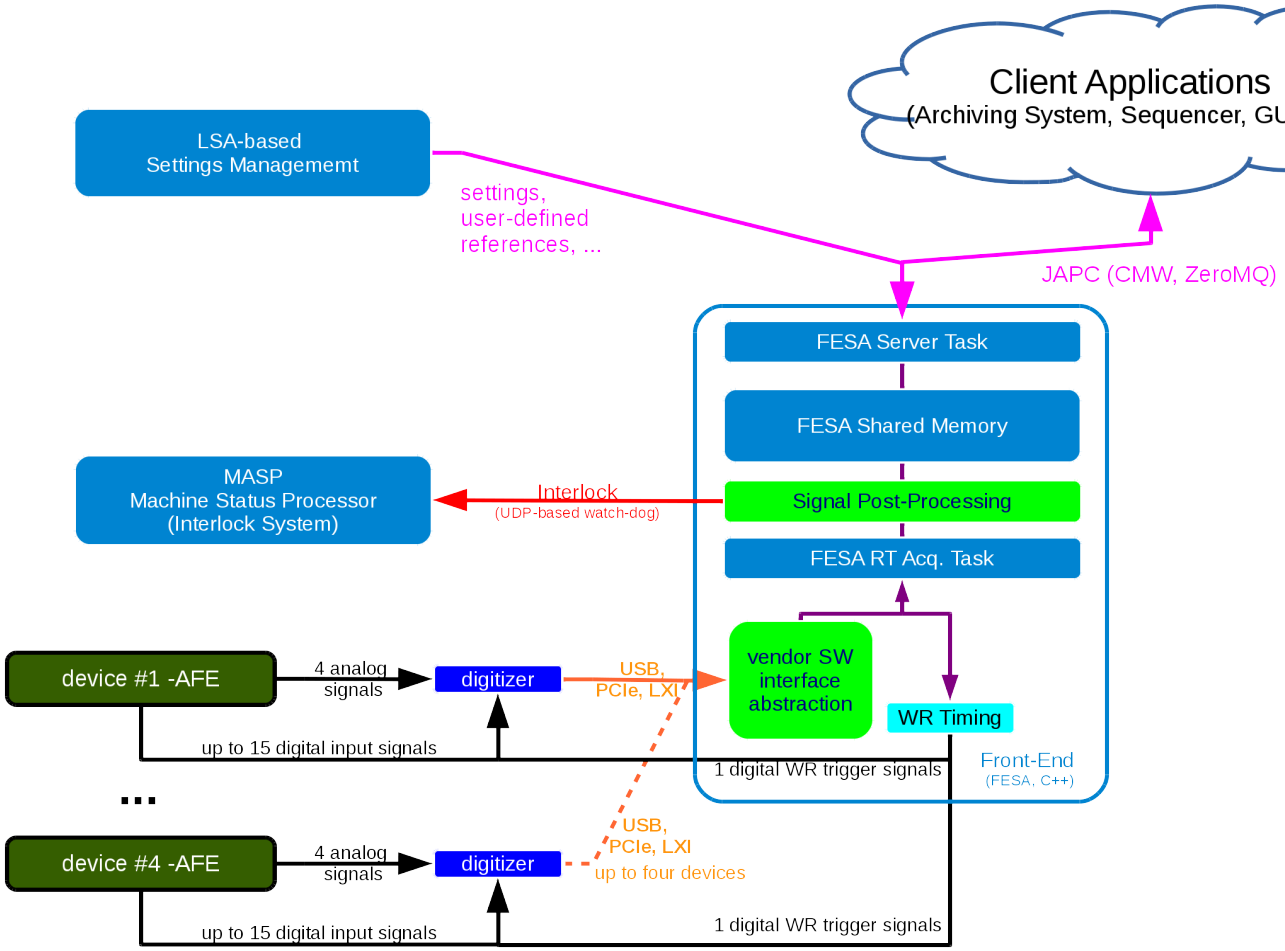
con:
- high-reconfiguration overhead (manual)
- limited test-coverage, trending

- targeted concept
  (underlying assumption: scopes/digitizers are cheap, RF switches are expensive)



permanent monitoring
(error-case, trending, interlocks, beam-based feedbacks, …)

Digitization of Analog Signals at FAIR and SIS18 in '18
Detailed Integration Specification → in-kind contract



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Document Title:	**On the Digitization of (generic) Analog Signals in the FAIR Accelerator Complex**
Description:	Detailed specification for the integration of time-domain digitizers with analog bandwidths and sampling frequencies ranging from DC to up to hundreds of MHz into the accelerator control system
Division/Organization:	FAIR
Field of application:	FAIR Project, existing GSI accelerator facility
Version	V 0.4

Abstract

This document describes the generic integration of time-domain digitizers with analog bandwidths and sampling frequencies ranging from a few MHz to hundreds of MHz. These digitizers shall provide generic monitoring and diagnostics of accelerator-related devices that otherwise do not require further dedicated IO control features, specific post-processing (e.g. fast feedback loops), or where these features are already handled through another existing infrastructure.

This specification aims at providing a generic abstraction of the vendor-specific digitizer software interfaces, a limited range of generic data post-processing on the acquired data, and integration of these devices into the FAIR control systems by providing FESA standardised software interfaces.

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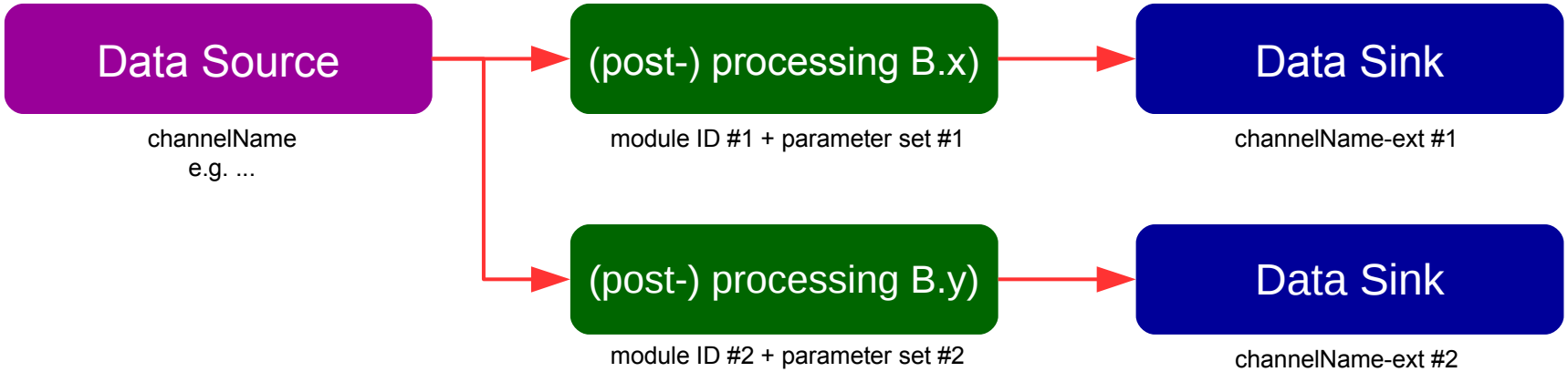
F-CS-C-0002e_Digitisation_of_Analog_Signals_v1.0.odt Hardcopy will not be controlled

released for formal approval tomorrow

General Signal-Flow Scheme

N.B. GNU-Radio real-time streaming processing inspired



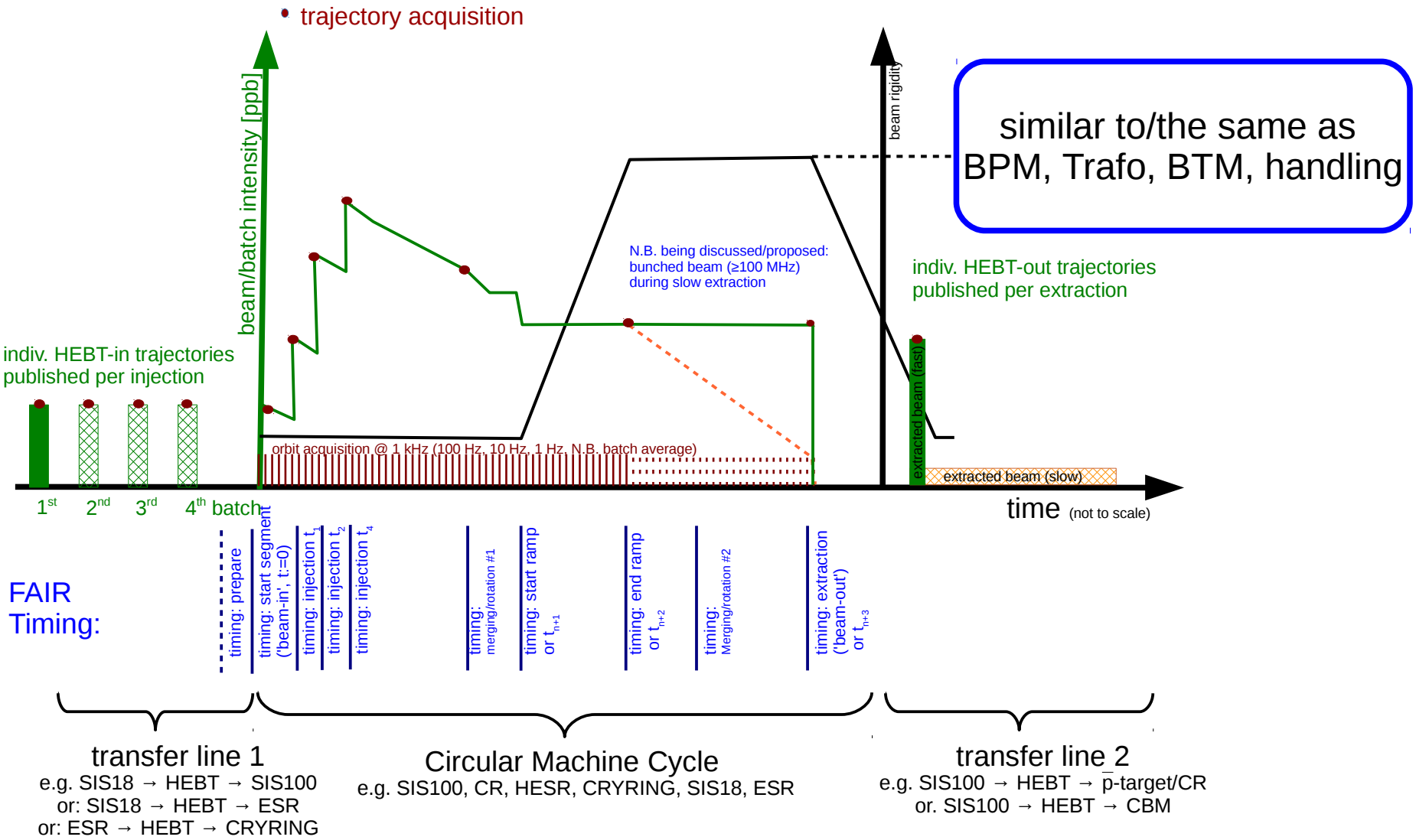
- Scheme can be further cascaded and combined with other modules
  - based on GNURadio‘s signal-flow concept https://www.gnuradio.org/
    - N.B. there are conceptually also other similar other projects: e.g. ADS, QUCS, Spice, LabVIEW … but with a different non-real-time (RF) signal processing

From the Specification (V 1.0)

https://edms.cern.ch/document/1823376/

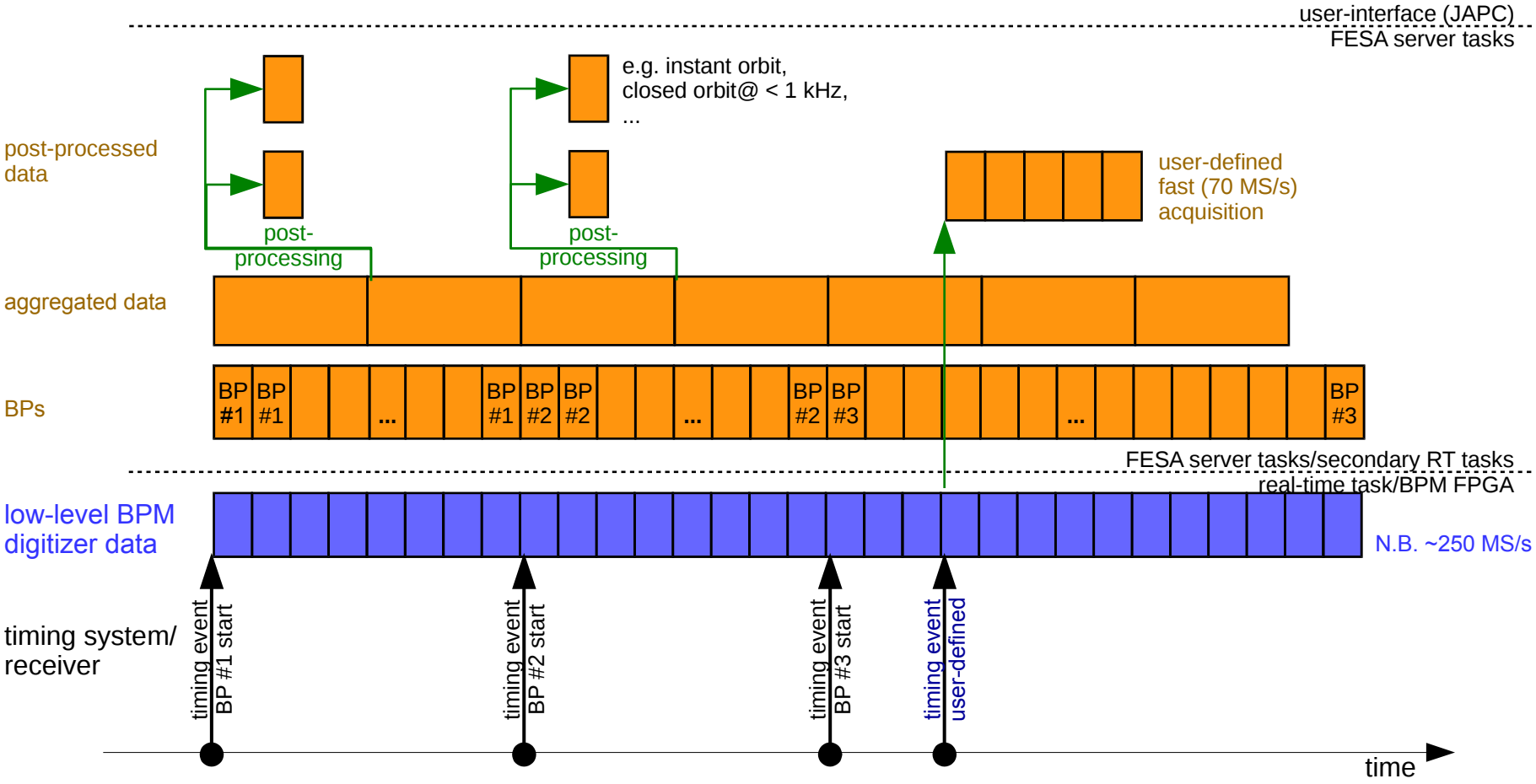
- Two data acquisition modes:
  - A.1) Streaming-mode acquisition
  - A.2) (Rapid) block-mode acquisition
- Limited set of post-processing modules:
  - B.1) raw-measurement scaling and offset shift
  - B.2) time-base re-alignment (lag & extr. event offset compensation)
  - B.3) data aggregation and decimation (typ. to kHz → Hz)
  - B.4) real-time Short-time Fourier Transform (STFT)
  - B.5) amplitude, phase and frequency detection (I-Q demodulation)
  - B.6) χ^2-type fitting and basic peak detection
  - B.7) actual versus reference comparison → interlock

Data Acquisition, Client Interfaces & Synchronisation



Low-Level Acquisition Modes
A.1) Streaming-mode acquisition I/II

acquisition schematic:



Generic Acquisitions I/II
Specified FESA Data Streams

Following modes of acquisition would be expected to be served simultaneously (though some of them could be implemented as down-sampled copies of the higher bandwidth acquisition):

A. Slow-acquisition (FESA property: 'Acquisition') – sub-choices (selected via CMW-filter):

1) **'Sequence'** acquisition between 'beam injection' and 'beam extraction': the specific signal averaged and decimated to the rate needed for the given client (e.g. 1 kHz).
   → *property notifies complete trace as a function of time at the end of the sequence (up to 30-60 s)*
2) **'Continuous'** real-time data publication during the cycle (↔N.B long SIS100 cycles and/or storage rings): → *property notifies single measurement at typical update rate around 10-25 Hz*
   - use-case: user-level applications (inj./extr. steering), software-based real-time feedbacks, ...
3) **'Instant'** signal acquisition: → *property notifies single measurement at pre-defined time delays (ms-scale)*
   - software interlock on injection/extraction orbit deviations (via MASP)

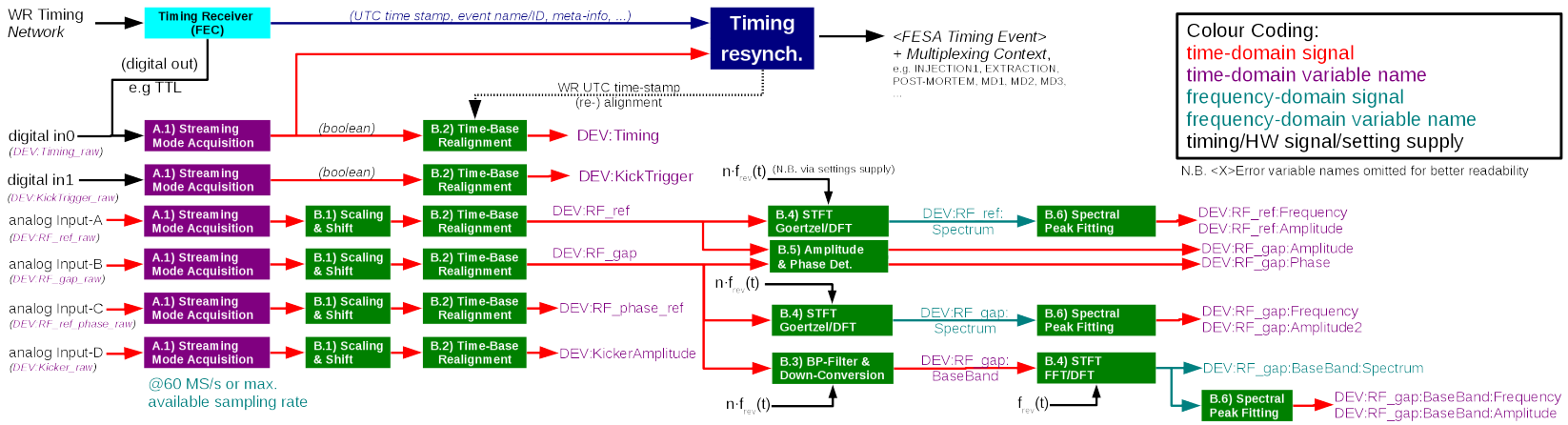
B. Fast block-mode acquisition (also 'Acquisition'):

- up to 10 external user-defined timing triggers per sequence (ie. each injection, extraction etc.)
  - corresponding CMW property subscription: e.g. 'TRIGGERED' or name of specific timing event
- horizontal channel settings are assumed to be fixed per digitizer

C. Post-Mortem (FESA property 'PostMortem'): not finalized but provisionally:

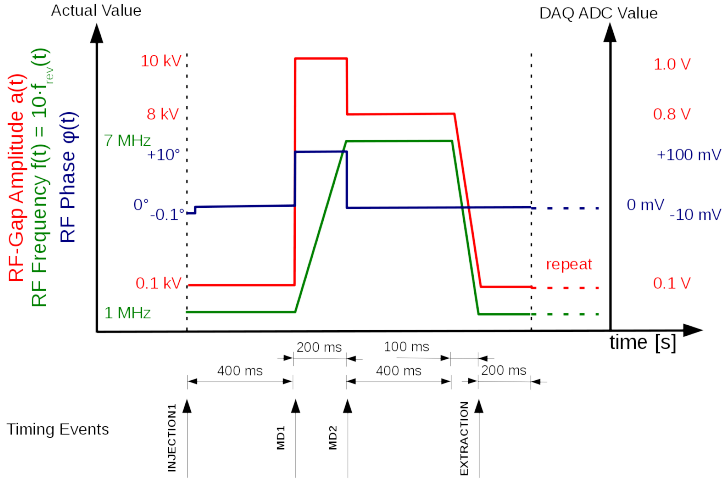
1) first circular buffer storing each signals @ 1 kHz for the last second of beam or full cycle
2) second circular buffer storing the last 1k (10k?) turns at maximum sampling rate

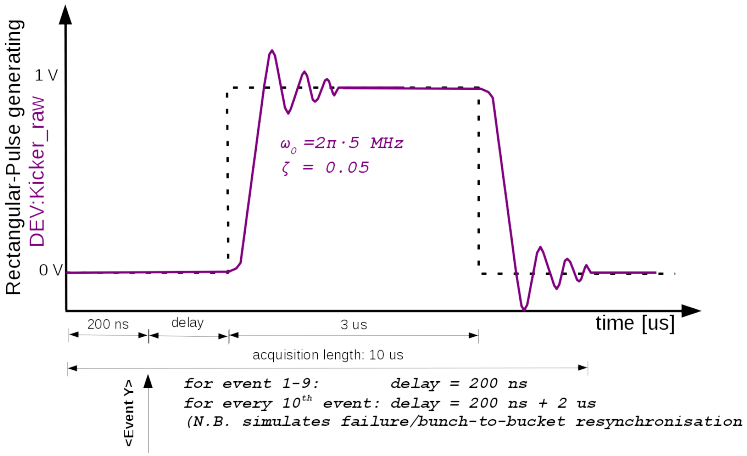
Signal Flow-Graph → SAT I/II



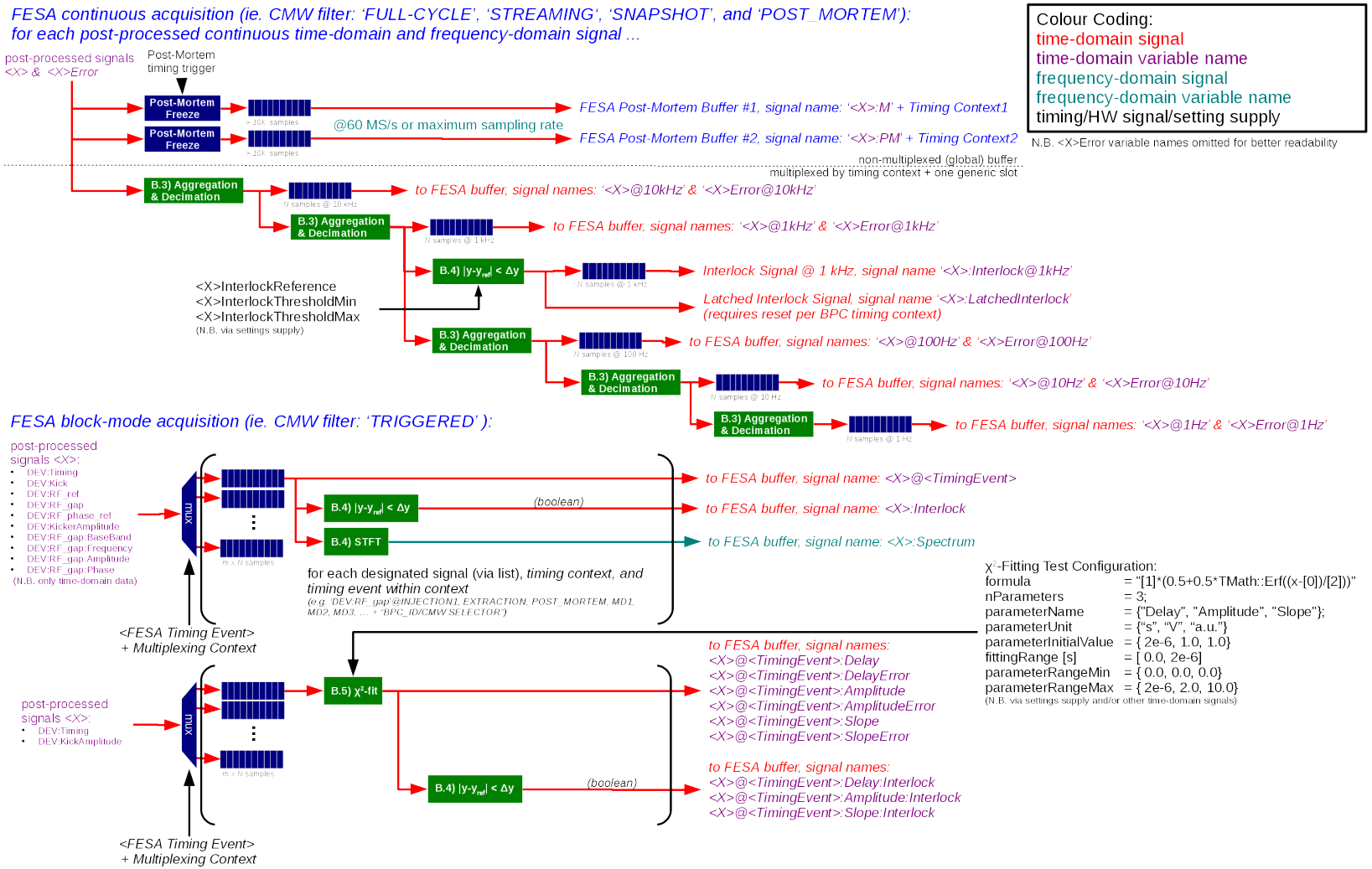
Test Signal Definition:

```
Analog Input-A: DEV:RF_ref_raw (t)     = '1 V'·sin(2π·[f(t) + φ(t)]) + '1% noise'
Analog Input-B: DEV:RF_gap_raw (t)     = a(t)·sin(2π·[f(t) + φ(t)]) + '1% noise'
Analog Input-C: DEV:RF_ref_phase (t)   = φ(t) + '1% noise'
Analog Input-D: DEV:Kicker_raw (t)     = 2nd-orderIIR(Rectangular-Pulse(t-t_event' <parameter see below>), ω_0=2π·5 MHz, ζ= 0.05)+ '2% noise'
```





Signal Flow-Graph → SAT II/II



Time- & Frequency-Domain Acquisition Interface

4.3.1 Time-Domain FESA Acquisition Properties User-Interface

Property	Variable Name	Brief Description	Variable Type	SI unit
Acquisition	selectedFilter	property filter for the selected 'Top-Level Acquisition Mode' (see Section 4.1 for details) & selected channel name	Enum + String[13]	
Acquisition	acqTriggerName	trigger name[14]	Enum	[]
Acquisition	acqTriggerTimeStamp	UTC trigger time-stamp	WR Time Stamp	[s]
Acquisition	acqLocalTimeStamp	time-stamp w.r.t. beam-in trigger	Integer (64 bits)	[s]
Acquisition	channelTimeBase	time scale	1D-array of integers	[s]
Acquisition	channelUserDelay	user-defined delay	float (32 bits)	[s]
Acquisition	channelActualDelay	actual trigger delay (i.e. during bunch-to-bucket transfer)	float (32 bits)	[s]
Acquisition	channelName	name of digitizer input or post-processed signals	String	[]
Acquisition	channelValue	value of digitizer input or post-processed signals	1D-array of floats (32 bits)	[channelUnit[15]]
Acquisition	channelError	r.m.s. error of post-processed signal	1D-array of floats (32 bits)	[channelUnit]
Acquisition	channelUnit	S.I. unit of post-processed signal	String	[]
Acquisition	status	status bit-mask	Integer	[a.u.]
Acquisition	temperature[16]	temperature of AFE, etc.	1D-array of floats (32 bits)	[°C]

↔ same style as other acquisition systems: BPM, Trafos, ...

4.3.2 Frequency-Domain FESA Spectrum Acquisition Property User-Interface

Property	Variable Name	Brief Description	Variable Type	SI unit
AcquisitionSpectra	selectedFilter	property filter for the selected 'Top-Level Acquisition Mode' (see Section 4.1 for details) & selected channel name	Enum + String[17]	
AcquisitionSpectra	acqTriggerName	trigger name	Enum	[]
AcquisitionSpectra	acqTriggerTimeStamp	UTC trigger time-stamp	Integer (64 bits)	[s]
AcquisitionSpectra	acqLocalTimeStamp	time-stamp w.r.t. beam-in trigger	Integer (64 bits)	[s]
AcquisitionSpectra	channelName	name of digitizer input or post-processed signals	String	[]
AcquisitionSpectra	channelMagnitude	magnitude specta of digitizer input or post-processed signals	1D-array of floats	[channelUnit /√Hz]
AcquisitionSpectra	channelMagnitude_dimensions	$\{N_{meas}, N_{binning}\}$	1D-array of integers	[]
AcquisitionSpectra	channelMagnitude_labels	{"time", "frequency"}	1D-array of strings	[]
AcquisitionSpectra	channelMagnitude_dim1_labels	timestamps of the samples	1D-array of long	[]
AcquisitionSpectra	channelMagnitude_dim2_labels	frequency scale	1D-array of floats	[Hz] or [f_{rev}]
AcquisitionSpectra	channelPhase	phase specta of digitizer input or post-processed signals	1D-array of floats	[rad]
AcquisitionSpectra	channelPhase_labels	{"time", "frequency"}	1D-array of strings	[]
AcquisitionSpectra	channelPhase_dim1_labels	timestamps of the samples	1D-array of long	[]
AcquisitionSpectra	channelPhase_dim2_labels	frequency scale	1D-array of floats	[Hz] or [f_{rev}]

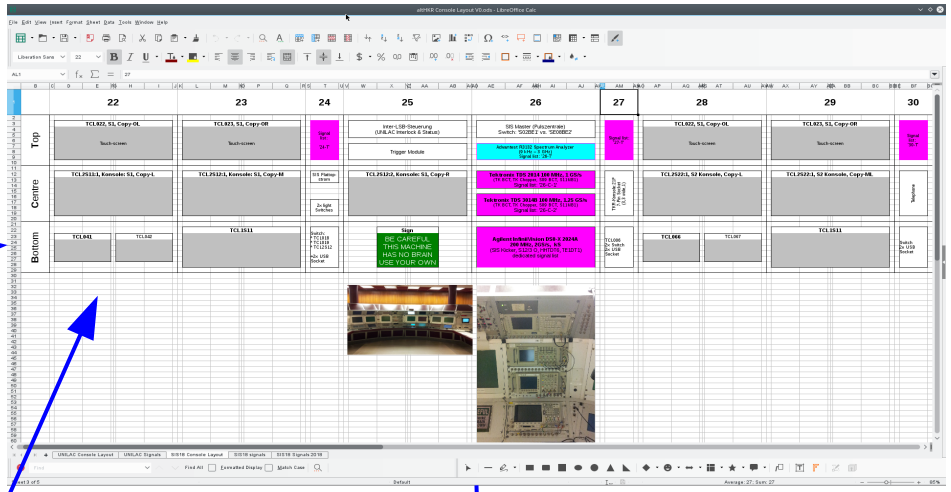
Table 2: Frequency-Domain FESA Acquisition Property for magnitude- and phase-spectra data.

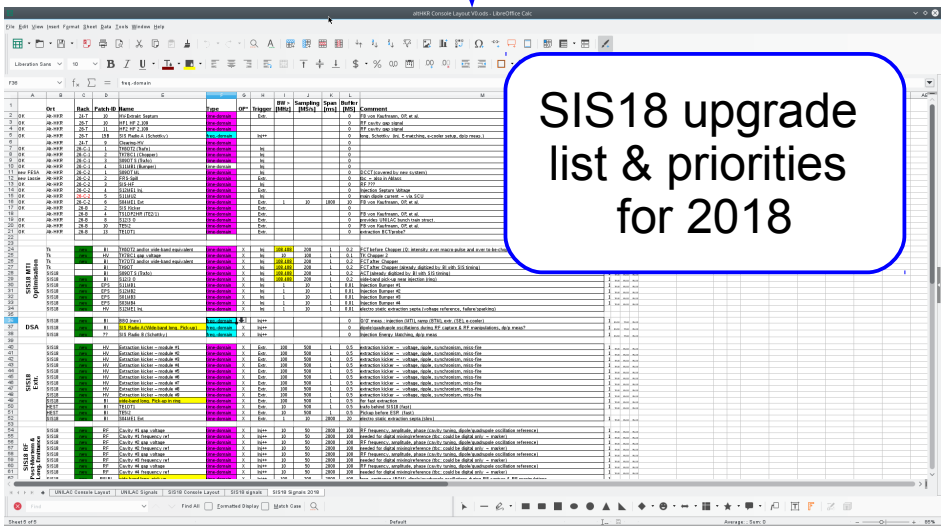
- Interface defined per 'signal' ie. signal name is part of subscription filter property
  - short term: full list of available signals via 'ChannelDescription' Property & Java API (2018)
  - long-term: 'name server' type service (upgradability/extension)

Documentation of Operational Usage
UNILAC & SIS18

Kaufmann, Reeg, Roedl, Steinhagen, Wiessmann et al.

Kaufmann, Steinhagen et al.





SIS18 upgrade list & priorities for 2018

2018 Digitizer Deployment & System Distribution
as agreed with MC & Controls

	Ort	Rack	Patch-ID	Quelle Raum	Quelle Rack	System ID	Digitizer Card	Name	Type	OP*	Trigger	BW > [MHz]	Sampling [MS/s]	Span [ms]	Buffer [MS]	Comment
SIS18 MTI Optimisation	Tk	OK	BI	LSB	12-15	#11	14	TK6DT2 and/or wide-band equivalent	time-domain	X	Inj	1	200	1	0.2	FCT before Chopper (Q: intensity over macro-pulse and over to-be-chopped pules)
	Tk		HV					TK7BC1 gap voltage	time-domain	X	Inj	10	100	1	0.1	TK Chopper 2
	Tk		BI					TK8DTx and/or wide-band equivalent	time-domain	X	Inj	1	200	1	0.2	FCT after Chopper
	Tk		BI	XX	XX			TK9DT	time-domain	X	Inj	1	200	1	0.2	FCT after Chopper (already digitized by BI with SIS timing)
	SIS18		BI					S09DT S (Trafo)	time-domain	X	Inj	1	200	1	0.2	ACT (already digitized by BI with SIS timing)
	SIS18	OK	BI	BG 2.009	44	#12	15	S12/3 O	time-domain	X	Inj		200	1	0.2	wide-band pick-up near injection (ring), rack responsible: Roland Fischer
	SIS18	OK	EPC	BG 2.002	17	#9	9	S11MB1	time-domain	X	Inj	1	10	1	0.01	Injection Bumper #1 (resp. Jürgen Trüller)
	SIS18		EPC					S12MB2	time-domain	X	Inj	1	10	1	0.01	Injection Bumper #2 (resp. Jürgen Trüller)
	SIS18		EPC					S01MB3	time-domain	X	Inj	1	10	1	0.01	Injection Bumper #3 (resp. Jürgen Trüller)
	SIS18		EPC					S03MB4	time-domain	X	Inj	1	10	1	0.01	Injection Bumper #4 (resp. Jürgen Trüller)
	SIS18	OK	EPC	BG 2.002	17		10	TK vertical bumper	time-domain	X	Inj	1	10	1	0.01	TK bumper (to be checked if needed by OP)
	SIS18	OK	HV	BG 2.002	18			S12ME1 Inj.	time-domain	X	Inj	1	10	1	0.01	electro static injection septa (voltage reference, failure/sparking)
DSA	SIS18	OK	RF	BG 1.016	6	#8	8	SIS Radio A (Wide-band long. Pick-up)	freq.-domain	X	Continuous				0	dipole/quadrupole oscillations during RF capture & RF manipulations, dp/p meas?
	SIS18	OK	BI	BG 2.009	110	#1	1	SIS Radio B (Schottky)	freq.-domain	X	Continuous*	50	70		0	Injection Energy Matching, dp/p meas
	SIS18	OK	BI	BG 2.009	110			BBQ (new)	freq.-domain	X	Continuous				0	Q/Q' meas.: injection (MTI), ramp (BTM), extr. (SE), e-cooler)
SIS18 Extr.	SIS18	OK	HV	RT 1.002	1.002	#10	11	Extraction kicker – module #1	time-domain	X	Extr	200	500	1	0.5	extraction kicker → voltage, ripple, synchronism, miss-fire
	SIS18	OK	HV					Extraction kicker – module #2	time-domain	X	Extr	200	500	1	0.5	extraction kicker → voltage, ripple, synchronism, miss-fire
	SIS18	OK	HV					Extraction kicker – module #3	time-domain	X	Extr	200	500	1	0.5	extraction kicker → voltage, ripple, synchronism, miss-fire
	SIS18	OK	HV					Extraction kicker – module #4	time-domain	X	Extr	200	500	1	0.5	extraction kicker → voltage, ripple, synchronism, miss-fire
	SIS18	OK	HV				12	Extraction kicker – module #5	time-domain	X	Extr	200	500	1	0.5	extraction kicker → voltage, ripple, synchronism, miss-fire
	SIS18	OK	HV					Extraction kicker – module #6	time-domain	X	Extr	200	500	1	0.5	extraction kicker → voltage, ripple, synchronism, miss-fire
	SIS18	OK	HV					Extraction kicker – module #7	time-domain	X	Extr	200	500	1	0.5	extraction kicker → voltage, ripple, synchronism, miss-fire
	SIS18	OK	HV					Extraction kicker – module #8	time-domain	X	Extr	200	500	1	0.5	extraction kicker → voltage, ripple, synchronism, miss-fire
	SIS18	OK	HV				13	Extraction kicker – module #9	time-domain	X	Extr	200	500	1	0.5	extraction kicker → voltage, ripple, synchronism, miss-fire
	SIS18	OK??	HV					Q-Kicker	time-domain	X	Extr	200	500	1	0.5	extraction kicker → voltage, ripple, synchronism, miss-fire
	SIS18	OK	BI	BG 1.016	6	#8	15	wide-band long. Pick-up in ring	time-domain	X	Extr	100	500	1	0.5	for fast extraction
	HEST	OK	BI	BG 2.009	44	#12	13	TE1DT1FD	time-domain	X	Extr	10	500	1	0.5	trafo behind SIS18 (fast)
	HEST	OK	BI	BG 2.009	48			TE5/2	time-domain	X	Extr	10	500	1	0.5	Pickup before ESR (fast)
	SIS18	OK	HV	RT 1.002 or BG 2.009	18	#9	12	S04ME1 Ext	time-domain	X	Continuous*	1	10	2000	20	electro static extraction septa (slow extraction)
SIS18 RF Post-Mortem & Long. Emittance	SIS18	OK	RF	BG 1.016	6 resp. 7 rack next to 9	#2	2	Cavity #1 gap voltage	time-domain	X	Continuous*	10	50	2000	100	RF frequency, amplitude, phase (cavity tuning, dipole/quadrupole oscillation reference)
	SIS18							Cavity #1 frequency ref	time-domain	X	Continuous*	10	50	2000	100	needed for digital mixing/reference (tbc: could be digital only → marker)
	SIS18	OK	RF			#3	3	Cavity #2 gap voltage	time-domain	X	Continuous*	10	50	2000	100	RF frequency, amplitude, phase (cavity tuning, dipole/quadrupole oscillation reference)
	SIS18							Cavity #2 frequency ref	time-domain	X	Continuous*	10	50	2000	100	needed for digital mixing/reference (tbc: could be digital only → marker)
	SIS18	OK	RF			#4	4	Cavity #3 gap voltage	time-domain	X	Continuous*	10	50	2000	100	RF frequency, amplitude, phase (cavity tuning, dipole/quadrupole oscillation reference)
	SIS18							Cavity #3 frequency ref	time-domain	X	Continuous*	10	50	2000	100	needed for digital mixing/reference (tbc: could be digital only → marker)
	SIS18	OK	RF			#5	5	Cavity #4 gap voltage	time-domain	X	Continuous*	10	50	2000	100	RF frequency, amplitude, phase (cavity tuning, dipole/quadrupole oscillation reference)
	SIS18							Cavity #4 frequency ref	time-domain	X	Continuous*	10	50	2000	100	needed for digital mixing/reference (tbc: could be digital only → marker)
	SIS18	OK	RF			#6	6	Cavity #5 gap voltage	time-domain	X	Continuous*	10	50	2000	100	RF frequency, amplitude, phase (cavity tuning, dipole/quadrupole oscillation reference)
	SIS18							Cavity #5 frequency ref	time-domain	X	Continuous*	10	50	2000	100	needed for digital mixing/reference (tbc: could be digital only → marker)
	SIS18	OK	RF		51	#7	7	BC gap voltage	time-domain	X	Continuous*	10	50	2000	100	RF frequency, amplitude, phase (cavity tuning, dipole/quadrupole oscillation reference)
	SIS18							BC frequency ref	time-domain	X	Continuous*	10	50	2000	100	needed for digital mixing/reference (tbc: could be digital only → marker)
	SIS18	OK	RF		6	#8	8	FCT/ wide-band long. pick-up	time-domain	X	Continuous*	100	200	2000	400	long. emittance (BQM), dipole/quadrupole oscillations during RF capture & RF manipul*
	SIS18							wide-band long. pick-up frev	time-domain	X	Continuous*	1	10	2000	20	pickup frev reference (can be digital only → marker)

- + all “AEG” power-supplies in BG2.002 (in conjunction with EPC/CO)
  - N.B. >2018: SIS18 MC (P. Spiller) requested budget to complete digitize all SIS18 non-ACU/legacy power-supplies (to be implemented after beam-operation) → in 2019: SIS18 should be fully digital & ready for moving operation to the new FCC
- + some prototype studies for Schottky diagnostics @ESR (Sanjari et al.) and @CryRing (W. Kaufmann et al.)
  … if time permits

Main Digitizer Selection Criteria I/II

… analysed digitizers from >54 companies for:

- Controls Integration (what concerns initially by CO-supported devices):
  - support/availability of Linux drivers, compliance with Linux driver standards, and tracking of mandatory kernel (and security) updates
  - no non-embeddable solutions ↔ significant resource overhead related to integration & maintenance. Primary issues related to Windows/oscilloscope-based options (also CERN experiences): 24h/7 reliability & IT security costs for the remote-controlled operation
    - N.B. some devices may not be reached at the installation site during the beam operation, > 100 systems total
  - minimization of the targeted system platform heterogeneities (minimisation of system/driver dissimilarities)

- Electrical and RF aspects (↔ based on existing system and accelerator operation analysis)
  - analogue bandwidths between 20 MHz, 200 MHz, up to at least 500 MHz
  - full RF AFE with selective gain and offset adjustment
  - >7 ENOB for high bandwidths and/or near thermal noise for lower bandwidths (→ 8-bit up to 16-bit digitizers)
    - better resolution and early detection of system errors and/or accelerator parameter drifts before these may potentially lead to faults with longer down-times
  - fast multiple triggering of measurements with dead times below 2 us
  - min. 1 preferred >8 external digital trigger/signal inputs (fast status detection of fast timing/RF feedback parameters)

- Numerical performance requirements:
  - real-time data streaming, bandwidths > 60 MS/s ↔ multi-user capabilities & enables easy SW-based post-processing (N.B. also availability of SW-savvy personnel vs. scarce VHDL expert resources at GSI/FAIR)
    - NB this being another exclusion criterion for Ethernet-based oscilloscopes
  - preferred USB 3.0 interface connection (bandwidth, scalability, long-lasting standard, interface costs, space constraints)
  - optional: possible modification of the digitizer FPGA firmware (↔ permits future extensions/pushing SW post-processing to HW)

- Mechanical form factor
  - stand-alone digitizer with a maximum of 19" width and 1U-height ↔ actual available space in the the planned rack/system locations

Main Digitizer Selection Criteria II/II

- Qualitative vendor criteria
  - products must (largely) be already available ↔ no R&D (re-commissioning risk minimisation)
  - proven long-term experience in T&M instrumentation
  - sustainable, adapted & consistently further developed product range ↔ minimisation of future heterogeneity
  - broad market coverage ↔ sustainable supply source for for re-orders & extensions
  - prefer manufacturers from the EU and/or FAIR members
  - no vendors targeting price dumping
- Digitizer Costs target (excl. FEC/timing related costs):
  - < 700 EUR/channel respectively 3000 EUR/system (consisting of 4 channels @ 200 MHz)
  - scalability for FAIR, not yet foreseen systems, upgrades, external non-acc users, ...

Final Vendor/Model Selection
PicoScopes from Pico Technology

- Low-Bandwidths (< 20 MHz)
  - PicoScope 4824, 7 (8) channels, 11.3 ENOB @ 20 MHz)
    - N.B. ~ 16 ENOB @ 10 kHz ($\Delta I/I_{max} \sim 10^{-5}$)
  - 2018: primarily used for EPC-related systems (→ 2018: “AEG”)
    - planned to digitize: I_{ref}, U_{ref}, I_{actual}, U_{actual}, ΔI, U_{int}, + 1 spare
    - 8th channel for WR timing synchronisation

- Medium-range Bandwidths (< 200 MHz)
  - PicoScope 3403D MSO ↔ 3406D MSO), 4 ch, 6.9 ENOB @ 200 MHz
    - N.B. ~ 7.9 (15) ENOB @ 10 MHz (10 kHz) ($\Delta U/U_{max} \sim 10^{-3}$ ($3 \cdot 10^{-5}$))
  - 15 (16) digital channels → triggering e.g. on fast RF loops states, etc.
  - 2018: primarily for Ring-RF (→ “Gap Voltage”) and HV-extraction kicker trigger acquisition

- High-Bandwidth (< 500 MHz, (1 GHz))
  - PicoScope 6402C↔ 6404C, 4 channel, 7.3 (7.9) ENOB @ 500 (200) MHz
  - 2018: primarily used for HV extraction and tune kicker waveform
- Open: specification for further digitizer devices
  - tentatively: Ettus Research SDR for spectra-related applications

N.B. Ordered/deploy 39 digitizer for 2018, pending 40 more for >2018 (SIS18 EPC upgrade)

19” Mechanical Digitizer Integration

- For 2018 this will be done in-house
  (too small quantity for supplier, but open for future orders/models)

Key-aspects (to be finalized):

- 19”-1U form-factor
- mechanical connector adaptation
- digital IO adapter board
  (e.g. trigger 2x10 pin→ Lemo (terminated))
- double-redundant PSU
  (e.g. Traco, >1 Mh MTBF each)
  - single-/split-connection to power network ↔ meet same FEC standard
- Health-Monitor-Interface (HMI)
  - for remote reset
  - simple non-OP control tasks
- Front-Panel labelling/etching etc.

Tentative Front-End Server Platform
choice of Accelerator Controls Group

HP Proliant DL 180 (380) Gen9++

- 2U height, disk-less (tbc.)
- high-performance options:
  - Xeon 2620V4, 2.1 GHz, 8 cores
  - single-/dual-CPU option

< 80 cm
to be confirmed

- Main reasons for choice:
  - high redundancy: ~ 1 Mh MTBF
  - low integration, administration & maintenance overhead
    (N.B. ILO integration for >150 server, limited personnel for routine maintenance tasks → optimisation of personnel resources)

Conclusions

- Main focus: generic acquisition and common post-processing of analog signals in the range of a few MHz to hundreds of MHz (in theory: also > GHz)
  - vendor-specific HW abstraction (→ future upgrades of newer version or different models)
  - two basic low-level acquisition modes: continuous & rapid block-mode
  - set of 6 post-processing modules
  - maintainability & testability (unit testing, testing, testing, ...)

- Next steps:
  1. ~~(informal) 'Engineering Check' via FC2WG (& in-kind partner)~~
  2. formal 'Engineering Check' via EDMS (↔ collection of signatures of those who gave feedback)
  3. formal 'EDMS Approval' (↔ collection of signatures, tomorrow)
  4. Integration contract being already prepared, SAT targeted Q4'17/Q1'18
  5. Specific deployment/preparation → Dec'17/Jan'18
  6. First early tests during Dry-Run in February/March 2018 (EPC "AEG" re-commissioning)

- Open Items (N.B. not just digitizer, but also other systems):
  - ~~handling of 3D-data structures in FESA: Japc, Archiving, …~~
  - transmission of extraction event meta-information (via timing message, data-supply, … ?)
    - staged not for 2018
  - 'Form' over 'Performance', but should define a minimum standard and practical upper-boundary (engineering margin)
    - parallelisms, FEC platform, ...
  - ...

Appendix