GOETHE
UNIVERSITÄT
FRANKFURT AM MAIN

B2B Transfer System for FAIR
(Conceptual Design [1])

03.06.2015

Presenter: Jiaoni Bai
Professor: Oliver Kester
Supervisor: David Ondreka, Dietrich Beck
Cooperator: Thibault Ferrand

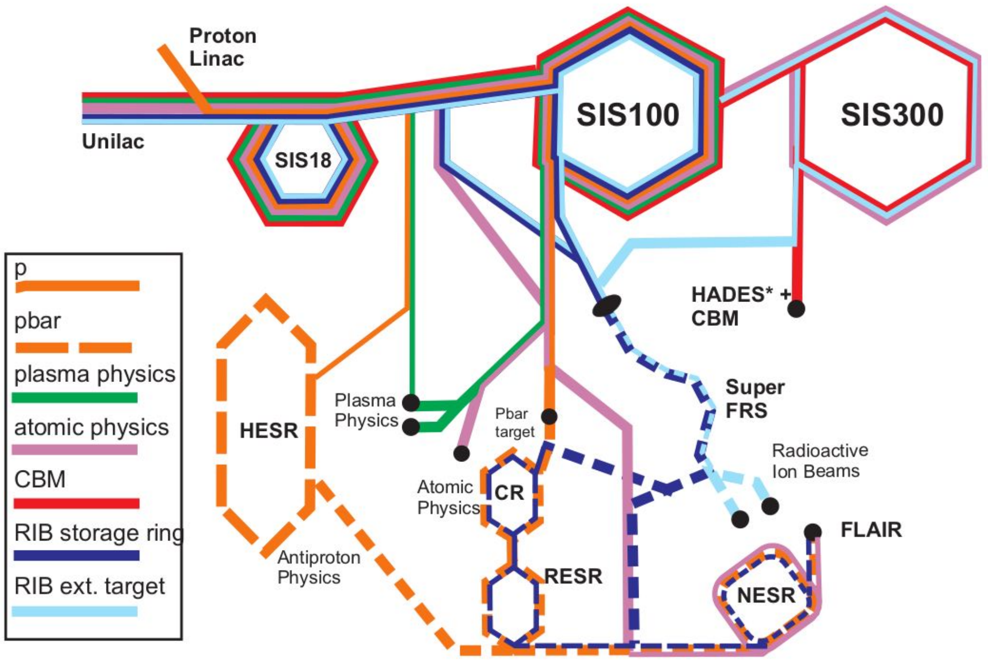
[1] https://edms.cern.ch/document/1514162/1

Outlines

- Purpose
- Synchronization methods
- Concept for the B2B transfer
- Standard procedures for the B2B transfer
- Architecture for the B2B transfer system
  - Functional block
  - Data/Signal flow
  - Component introduction
- Component specification

Purpose

The FAIR is aiming at providing high-energy beams with high intensities.
GSI existing accelerators: UNILAC, SIS18 and ESR
FAIR new accelerator complex: SIS100, CR and HESR.



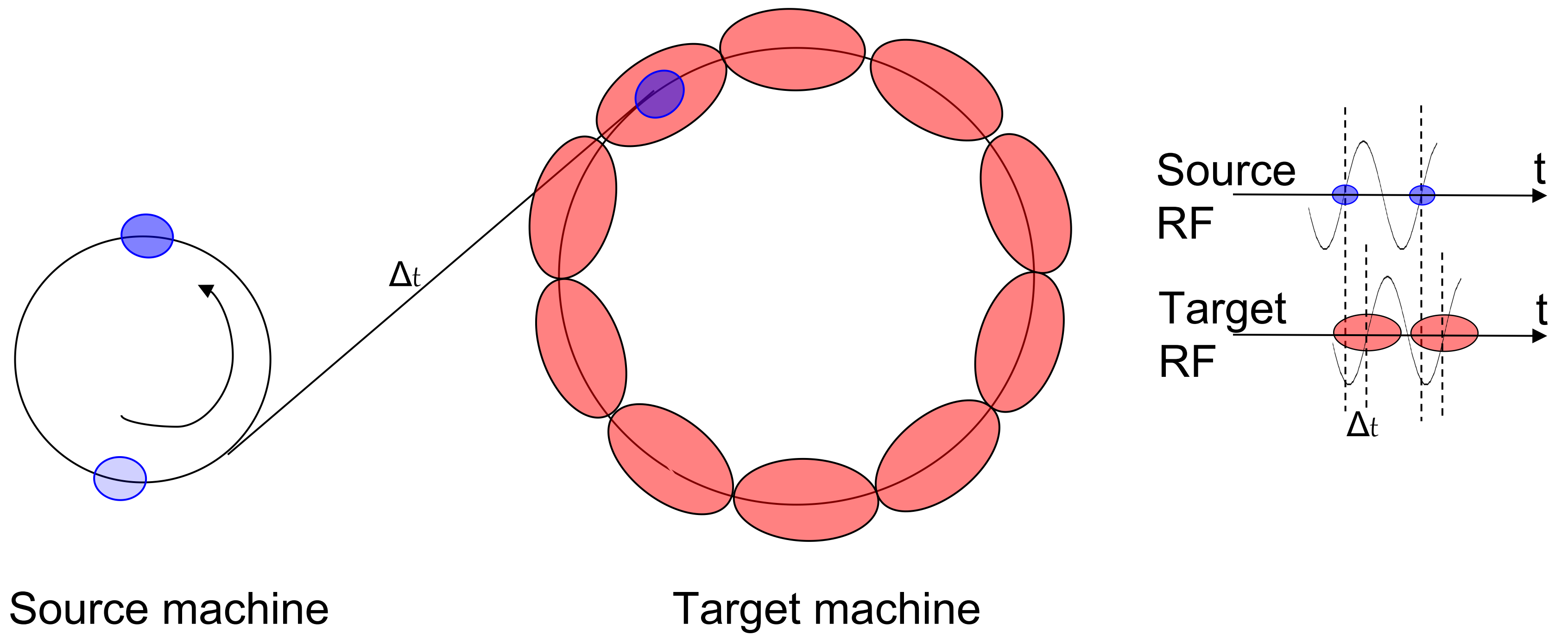
- The B2B transfer from the SIS18 to the SIS100
- The B2B transfer from the SIS18 to the ESR
- The B2B transfer from the SIS100 to the CR
- The B2B transfer from the CR to the HESR
- . . .

Purpose

Bucket: Stable phase space area where beam may be captured and accelerated [2] => stationary bucket

Bunch: A group of particles captured in a phase space bucket [2] (synchrotron)

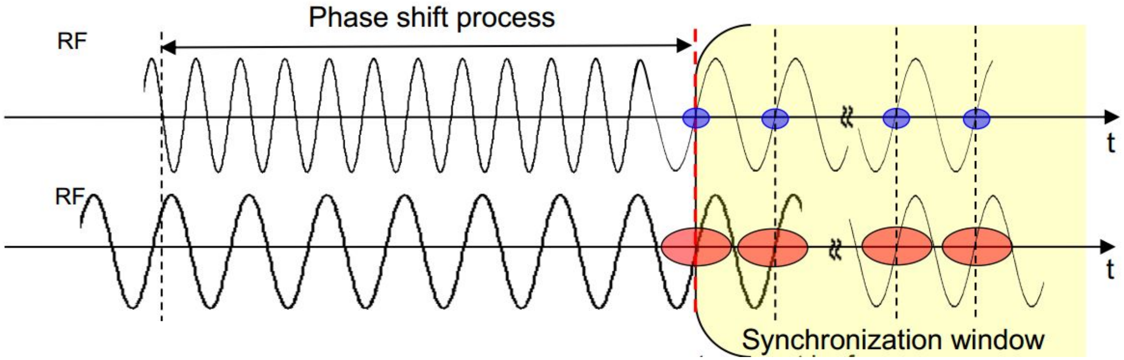
« **Bunch-to-Bucket transfer**» means that one bunch, circulating inside the source synchrotron, is transferred into the center of a bucket of the target synchrotron.



[2] Fermilab, Accelerator Glossary of Terms

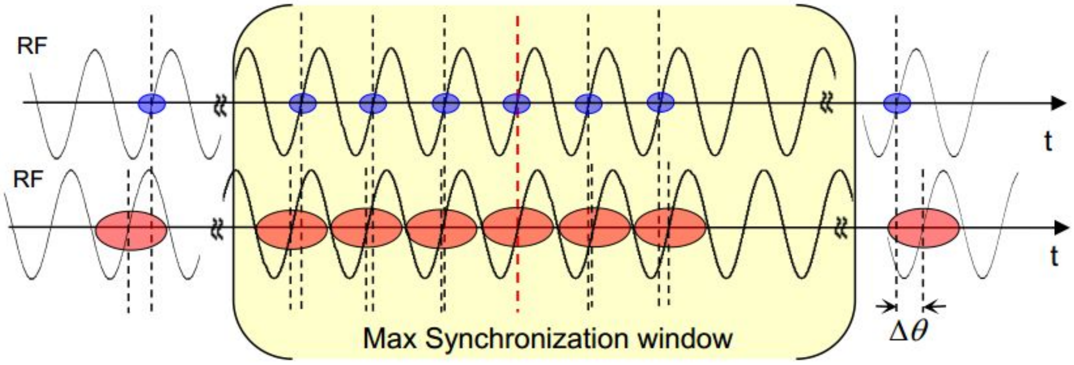
Synchronization methods

- Phase shift method (Here: phase shift only in source synchrotron and TOF = 0)



- RF flattop
- Infinite synchronization window in the ideal situation
- Adiabaticity

- Frequency beating method

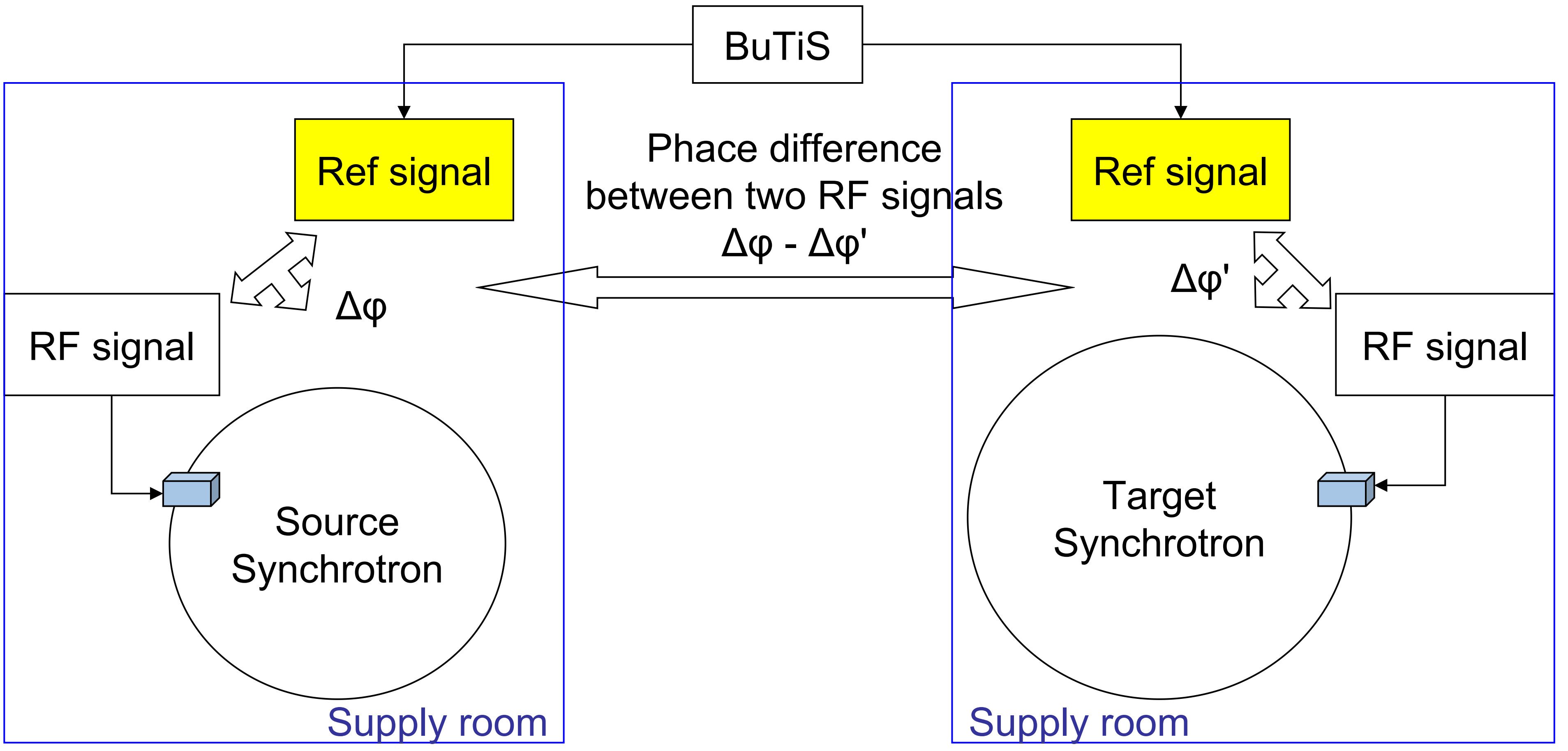


- RF ramp
- Mismatch bunch & bucket
- Synchronization window better than 1°
- Finite symmetric synchronization window

For CERN and other accelerator facilities, they have a preference for the phase shift method. For FAIR, the frequency beating method is also possible.

Concept of B2B for FAIR

- CERN and other accelerator facilities: the B2B transfer system is based on the cavity measured signal
- FAIR: the B2B transfer system is based on the driven signals derived from the BuTiS



Standard procedures

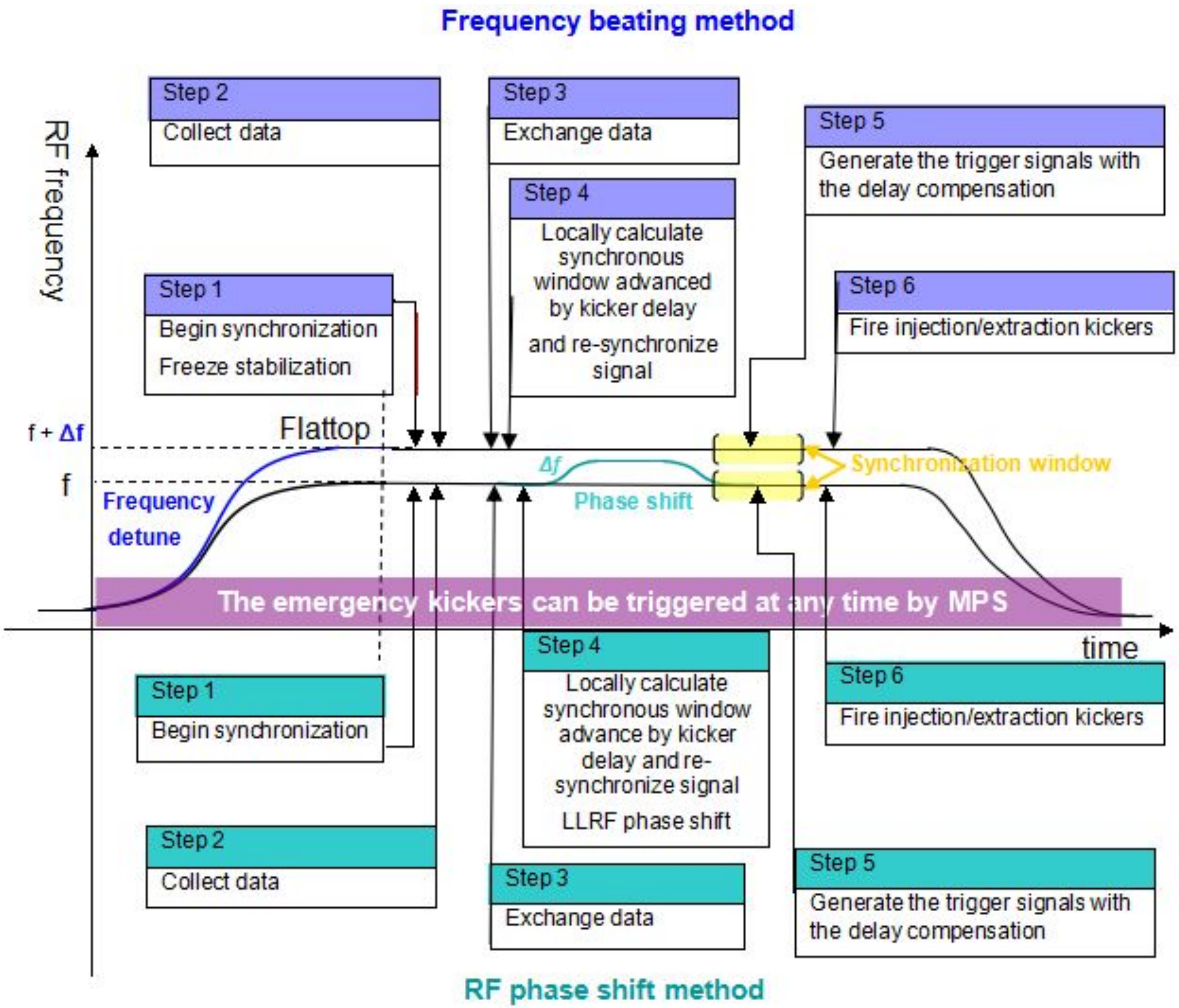


Figure 3: The procedure for the B2B transfer within one acceleration cycle

Architecture

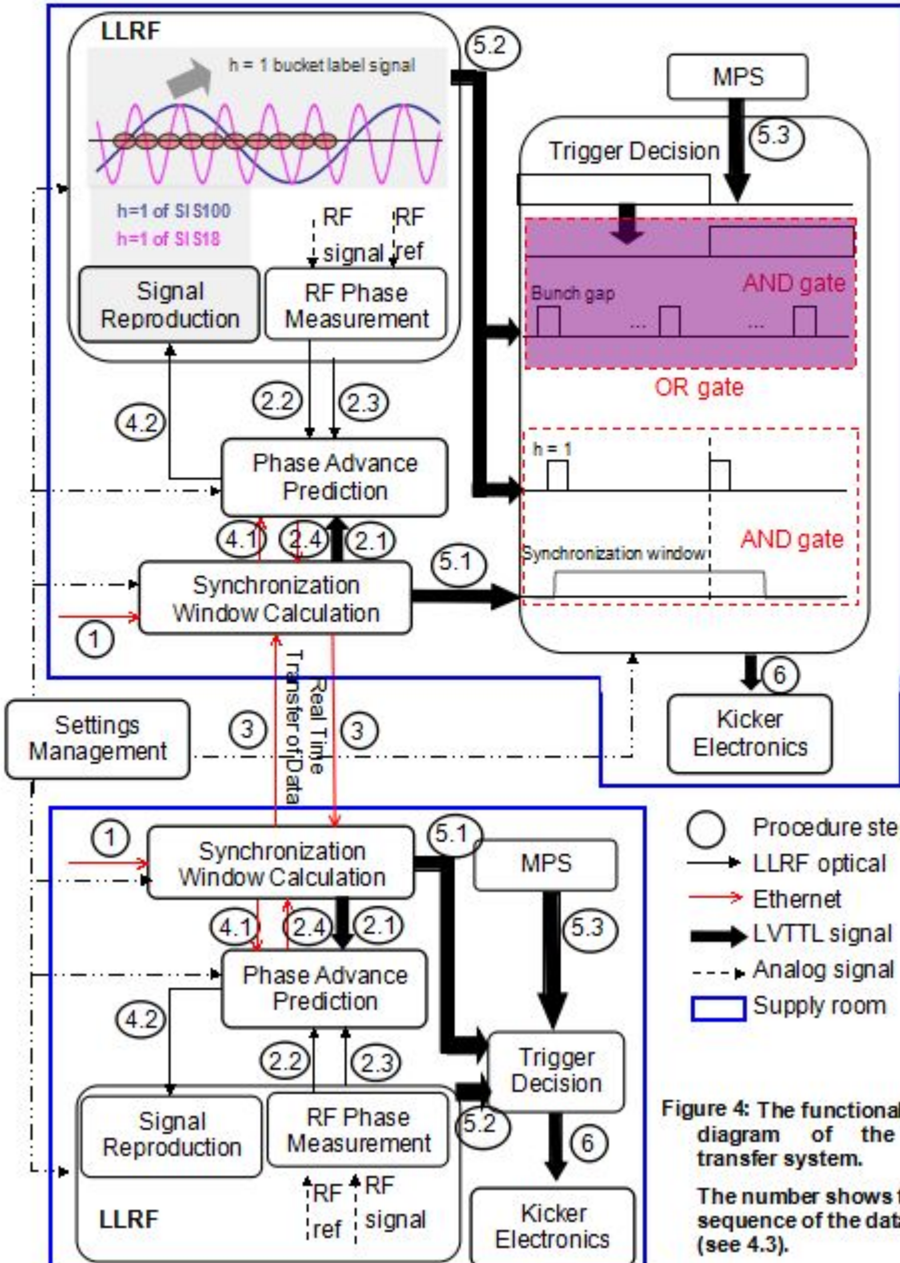


Figure 4: The functional block diagram of the B2B transfer system.

The number shows the sequence of the data flow (see 4.3).

- ➢ ***RF Phase Measurement Module***
  - Phase difference measurement
- ➢ ***Phase Advance Prediction Module (PAP)***
  - Phase difference prediction at any time
  - Data transmission between the SWC module and the LLRF system
  - Synchronized to the BuTiS T_0 and C2
- ➢ ***Signal Reproduction Module***
  - RF signals h = 1 duplication
  - RF phase correction
  - Provide bucket label signal (e.g. SIS100 h=1)
- ➢ ***Synchronization window calculation (SWC)***
  - Data exchange with PAP
  - Date exchange with the other synchrotron
  - Calculate the synchronization window
- ➢ ***Real time data transfer***
- ➢ ***Trigger decision module***
  - Normal extraction/injection kicker signal
  - Emergency kicker signal (Only SIS100)
- ➢ ***Kicker electronics***

Data/Signal flow

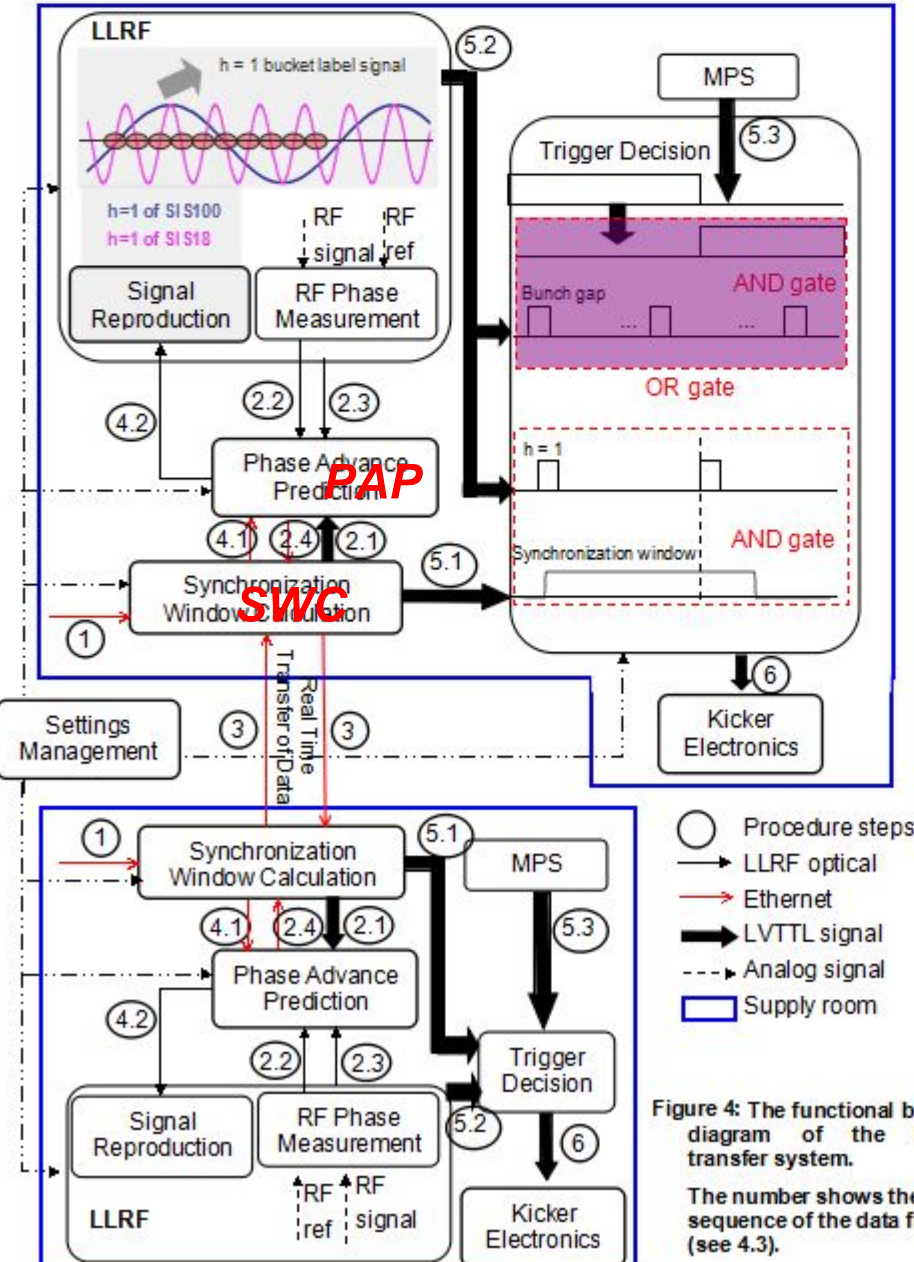


Figure 4: The functional block diagram of the B2B transfer system.

The number shows the sequence of the data flow (see 4.3).

Step 1. The DM announces the timing event for the B2B transfer.

Step 2. Once the SWC module receives this event.

2.1 It triggers the PAP module to collect data at the designated time.

2.2 The PAP module continuously gets the phase difference from the RF phase measurement module and it predicts the phase difference ΔΦ after a delay, which is N times of the BuTiS T_0 period.

2.3 The PAP module gets the RF frequency f_{rf} from the LLRF System.

2.4 The PAP module transfers data ΔΦ, f_{rf} and N to the SWC module.

Step 3. The SWC modules exchange the collected data between two synchrotrons via the WR network.

Data/Signal flow

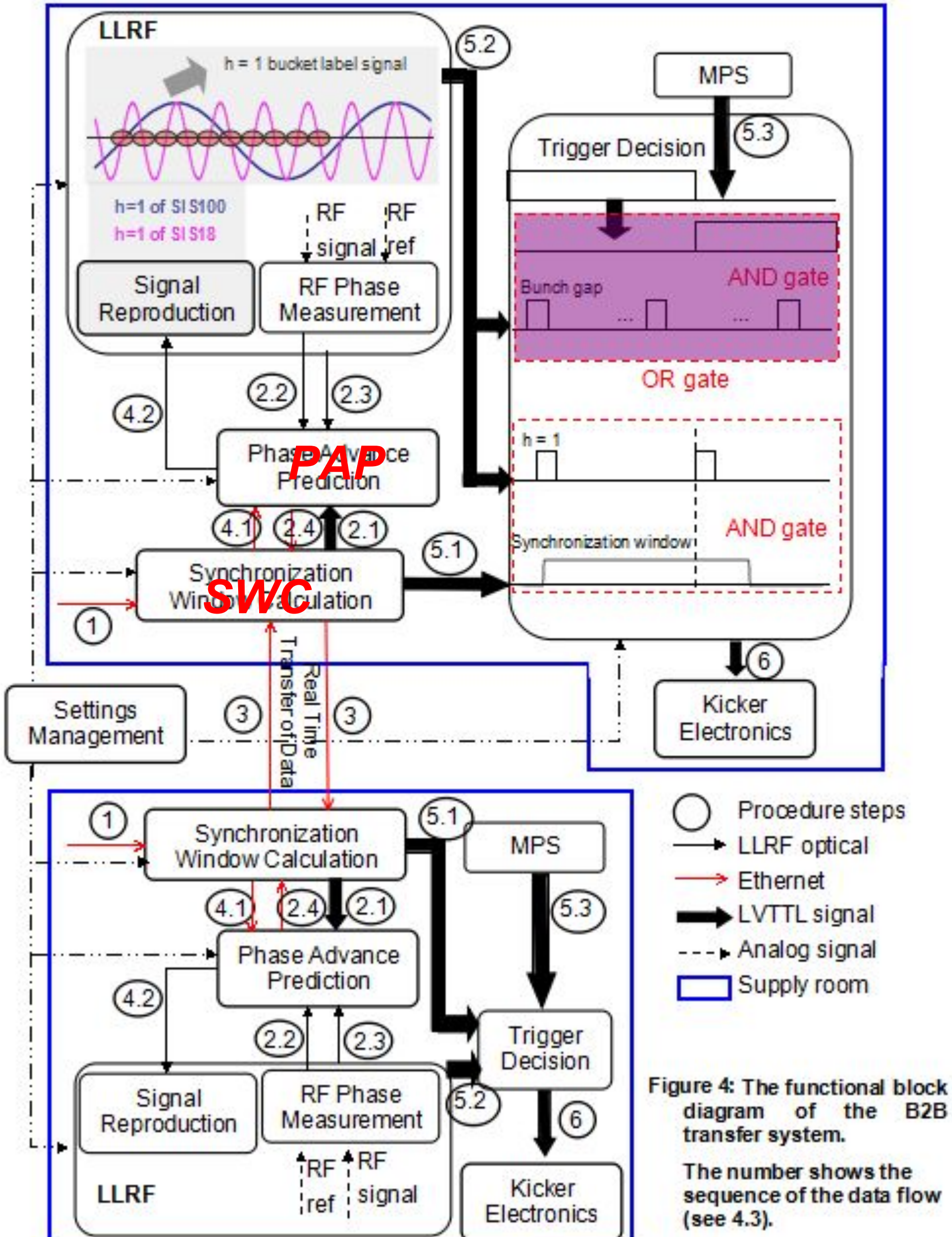


Figure 4: The functional block diagram of the B2B transfer system.

The number shows the sequence of the data flow (see 4.3).

Step 4. Once the SWC module of one synchrotron receives the data from the other synchrotron, it calculates the synchronization window locally.

4.1 The SWC module transfers the RF phase information ΔΦ' to the phase advance prediction module.

4.2 Then the PAP module transfers the phase information ΔΦ' to the signal reproduction module to correct RF phase.

Step 5. The trigger decision module produces the trigger signal for kickers.

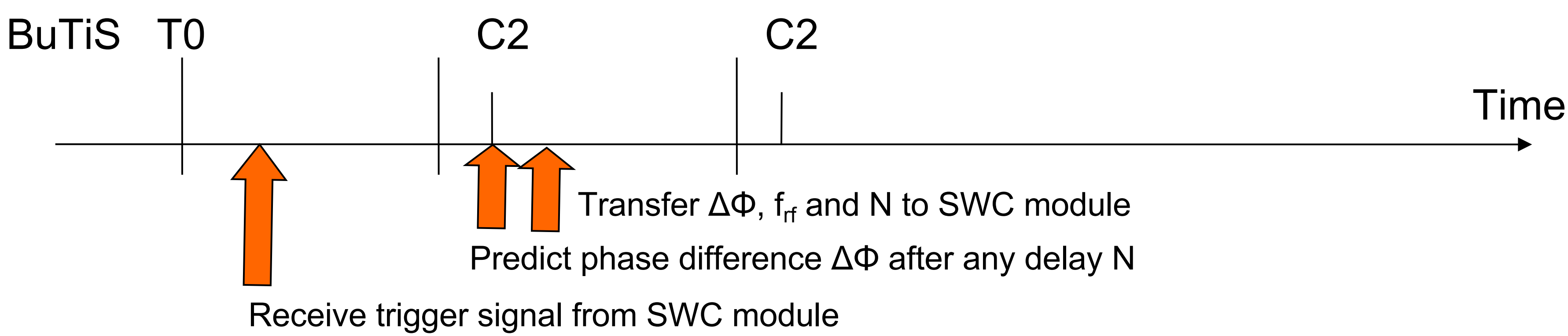
5.1 Synchronization window

5.2 Bucket pattern signal h = 1

5.3 MPS signal

Step 6. After receiving the trigger signal, the kicker electronics fires the kickers.

Phase advance prediction module



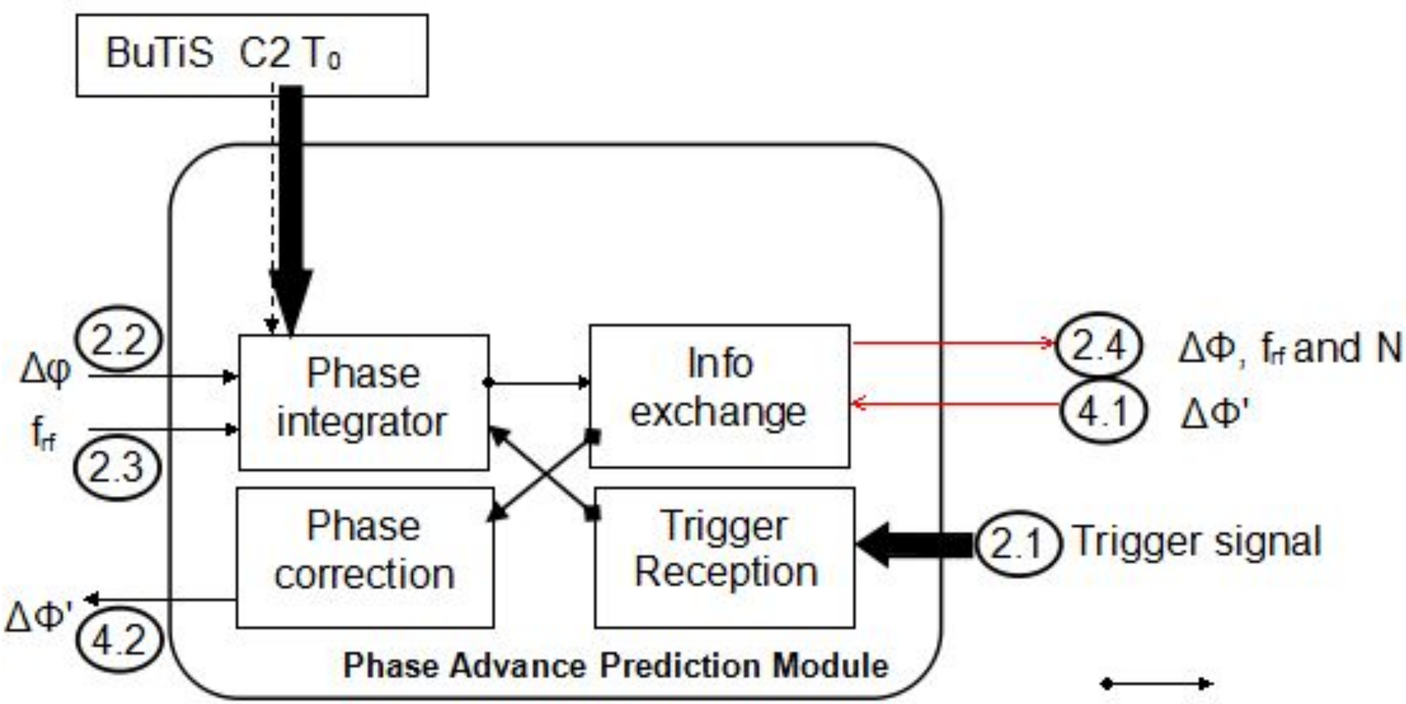
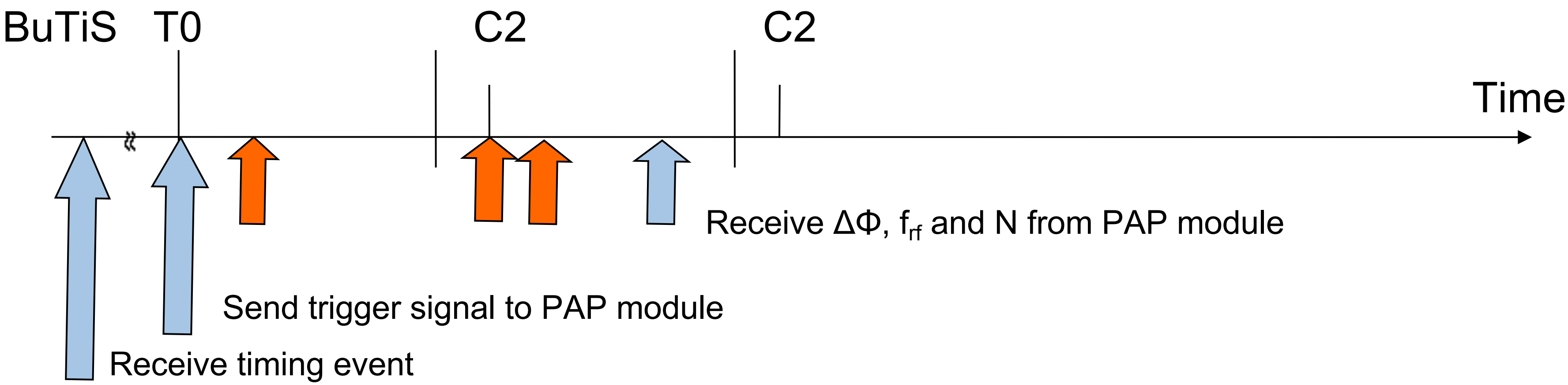


Figure 5: The phase advance prediction module

Synchronization window calculation module



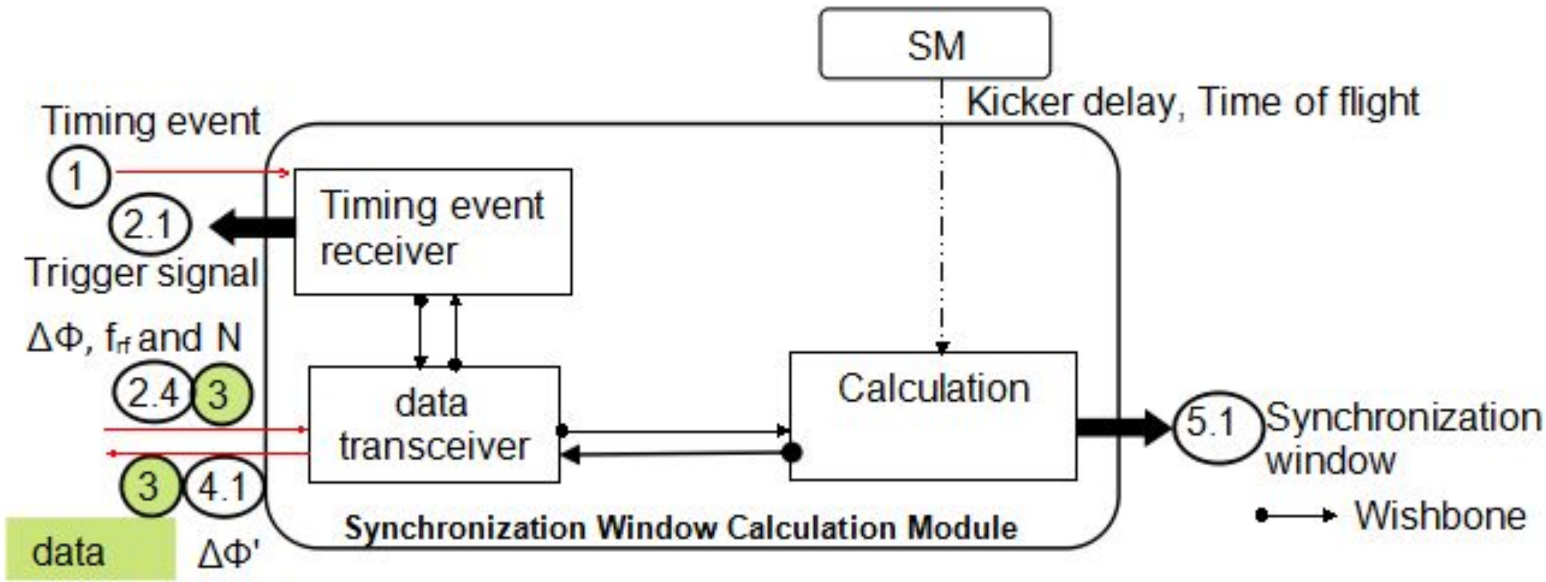


Figure 6: The synchronization window calculation module

Trigger decision module

The trigger decision module chooses the first TTL pulse of h = 1 within the synchronization window and delays this pulse by the compensation delay from the Settings Management (SM).

Kicker delay compensation

Including all the delays in cables, electronics, kicker preparation time.

Bucket pattern delay compensation

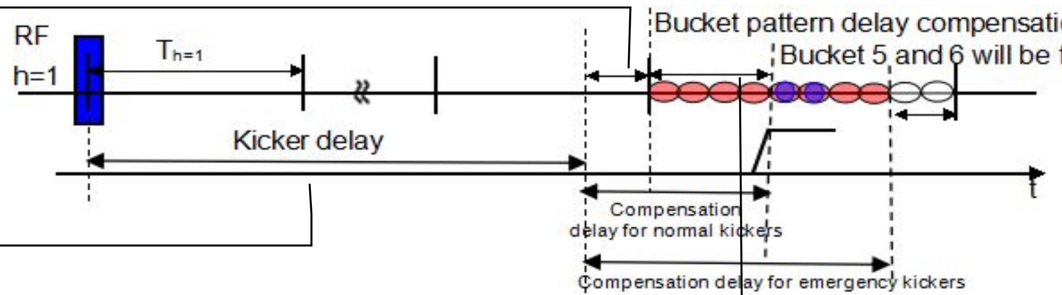


Figure 9: The illustration for the compensation delay with the bucket pattern of the SIS100 injection kicker and the compensation delay for the emergency kicker

For the emergency kicker, the compensation delay consists of the kicker delay compensation and bunch gap compensation.

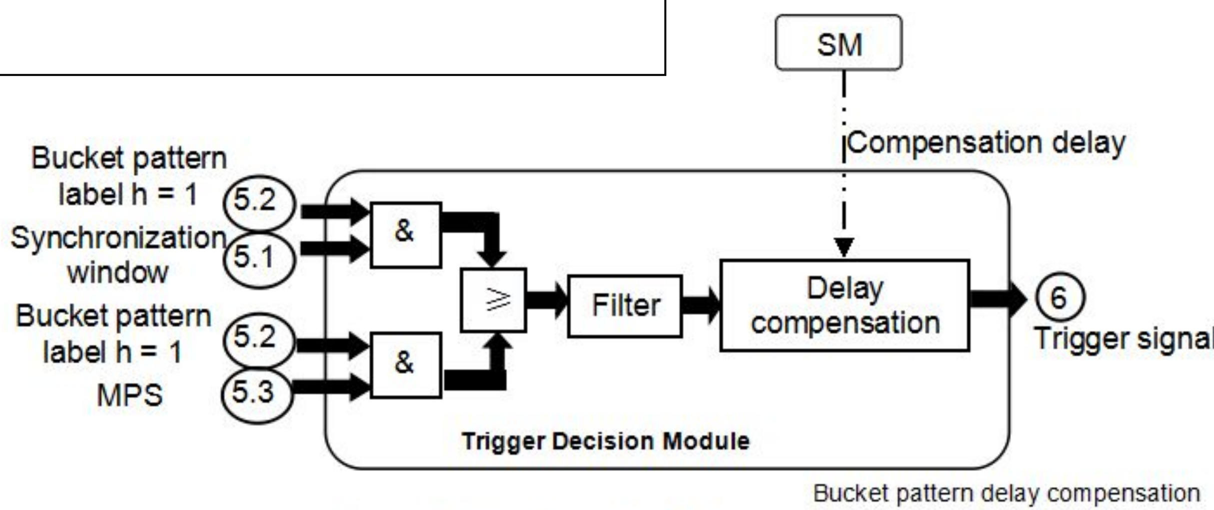


Figure 8: The trigger decision module

Component specification

Component name		Component specification	
RF Phase Measurement Module	PBRF	Direct Signal Processing (DSP) system (LLRF)	Measurement accuracy better than ±0.1°; measurement at the rate of 3.22 us; 1 optical direct link (ODL) output
Phase Advance Prediction Module	PBRF	Open issue	BuTiS T_0 and C2 Input; 2 ODL Input; 1 ODL Output; 1 Ethernet Input/Output (recommend)
Signal Reproduction Module	PBRF	Direct Digital Synthesis (DDS) module (LLRF)	RF generation (0.1 MHz - 27 MHz) with the resolution better than 2 Hz; RF <10 MHz integrated phase error less than 0.5° over 10 s; 1 ODL Input; 2 LVTTL Output
Synchronization Window Calculation Module	CS	Timing Receiver (TR) with new features	2 Ethernet Input/Output; 2 LVTTL Output; 1 FESA Input
Real Time Data Transfer	CS	WR network	Max latency via DM ≈1ms; Max latency via one WR switch ≈100 ~ 200 us
Trigger Decision Module	CS	Open issue	4 LVTTL Input; 1 LVTTL Output; 2 FESA Input
Kickers Module			1 LVTTL Input

Thank you for your attention!